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Strategies for enhancing DC gain and settling performance of amplifiers

by

Jie Yan

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This is to certify that the doctoral dissertation of

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Signature was redacted for privacy.

Major Professor

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For the Major Program

To my mother

To the memory of my father

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CHAPTER 1. INTRODUCTION

Amplification is an essential function in many analog and digital circuits. The operational amplifier (op amp) serves as the fundamental element for versatile amplifier functions [1]. Op amps are amplifiers that have sufficiently high forward gain so that when negative feedback is applied, the closed-loop transfer function is practically independent of the gain of the op amp. This principle has been exploited to develop many useful analog circuits and systems. Ideally, an op amp has infinite differential-voltage gain, infinite input resistance, and zero output resistance. In reality, an op amp only approaches these values. There are so many design parameters of op amps that are important in different applications. For example, DC gain, gain bandwidth, settling time, slew rate, output swing, offset, noise, common-mode input range, common-mode rejection ratio (CMRR), and power–supply rejection ratio (PSRR) etc. In practice, it is impossible to optimize all of these parameters simultaneously because most of these parameters trade off with each other. Depending on applications, op amps may be selected for speed, for noise, for input offset voltage, for common–mode range etc.. Different circuit architectures and manufacturing processes optimize different performance parameters.

The op amp is one of the most widely used and important building blocks in analog circuit design. High gain and high speed are two of the most important properties of op amps because they determine the settling behavior of op amps. Many analog and mixed signal systems have performance that is limited by the settling behavior of op amps. These include switched capacitor filters [2][3][4], algorithmic A/D converters, sigma-delta converters, sample and hold circuits [5][6], and pipelined A/D converters [7][8][9]. In these circuits the settling behavior of the op amp determines the accuracy and the speed that can be reached. For example, the major source of error in the pipelined A/D

converter that limits performance at higher frequencies is the incomplete settling of the inter-stage amplifiers. The incomplete settling of the inter-stage amplifier is almost entirely attributable to the characteristics of the op amp. Two factors are generally recognized as the contributors to the incomplete settling of the operational amplifier. One is the magnitude of the DC gain of the op amp, A_0. The gain must be high enough so that the DC gain with feedback, $A_f(0)=A_0/(1+\beta A_0)$ is sufficiently close to $1/\beta$ so that the resultant error is within a prescribed error budget of somewhat less than 1/2LSB when amplifier has settled. The second is attributable to the frequency response of the amplifier and its corresponding impact on the time it takes for the amplifier to settle when an input is applied.

Three research thrusts will be presented in this dissertation. The first focuses on the design of high gain operational amplifiers using a new negative conductance gain enhancement strategy. This is the major contribution of this research initiative and the ideas proposed are validated with experimental results obtained from test circuits that were designed and fabricated. The second thrust is directed towards the development of a new feedforward amplifier compensation strategy. Results are obtained from behavioral level simulations. The third thrust is directed towards a new asynchronous method for clock and data recovery in serial channel communications. A brief introduction to each of these three thrusts follows.

1.1 Research Motivation

1.1.1 High gain amplifiers

As supply voltages decrease when device feature sizes are reduced, the realization of high gain amplifiers with large Gain-Bandwidth-Products (GBW) has become challenging. As the power supply voltages go down, not all design principles used in the past can be directly translated to a lower voltage environment. Reducing the power supply voltage to a typical op amp has a number of

effects. Obviously, the signal swings both at the input and output are reduced. While this reduction does not normally increase noise levels in the system, signal-to-noise ratios will be degraded with reduced signal levels..

There are two conventional approaches to achieving low frequency gain boosting for standard CMOS processes. In the multi-stage op amp structure, a large DC gain can be achieved by cascading several low gain stages. Since the individual stages are not required to have high gains, the stages can more readily be designed to operate at very low voltages. For example, a cascaded amplifier could be constructed using standard differential amplifier stages that can operate under a supply voltage as low as 3 V_{dsat} drops for early stages in the cascade. Without significantly compromising the PSRR or CMRR, the output stage can be realized with a common-source amplifier that requires a minimum supply of 2 V_{dsat} drops plus the required signal swing. Arbitrarily high levels of voltage gain are achievable even in processes with substantial MOS drain conductance degradation. Although high DC gain is achievable with cascading, the accompanying excess phase shift introduces serious compensation requirement which limits the high frequency performance of cascaded amplifiers in feedback applications. In most of the published work, the compensation requirements have limited this approach to low frequency applications [12][13][14][15][16][17]. The energy efficiency of the reported structures is also not particularly attractive. The second conventional approach is based upon a single op amp stage structure in which gain enhancement is achieved by increasing the output impedance. Two techniques can be used to increase the output impedance. One is the cascoding technique. A second is the negative output impedance compensation technique.

The cascoding technique includes telescopic cascoding [18], folded cascoding [19][20], and regulated cascoding [10][21]. Cascoding topologies that exploit "stacking" of transistors were widely used in the past to achieve a high DC gain but they suffer from a limited output swing. With one level

of cascoding, there are 5 V_{dsat} drops in addition to the signal swing that must appear between the supply rails. The folded-cascode offers a modest signal swing improvement with 4 V_{dsat} drops rather than 5 V_{dsat} drops but suffers a modest degradation in the maximum speed of operation and is somewhat less energy efficient for a given settling requirement. Neither are attractive for low voltage operation. Neither have adequate gain for higher-resolution requirements and the gain will get worse as go degrades in the sub 100nm processes. The regulated cascode amplifier or now often termed the gain-boosted cascode amplifier can be applied to either the telescopic cascode or folded-cascode structure and has received considerable attention in recent years. This amplifier offers the advantage of a substantial boost in the dc gain over what was achievable with either the telescopic or folded cascode structures but it also only exhibits modest degradations in settling time and energy efficiency. Gain-boosting does not significantly affect the signal swing capabilities of the structures. In an attempt to improve the signal swing while still maintaining a large dc gain, Gulati and Lee [18] proposed what they termed the High-Swing Telescopic Cascode. In their approach, they biased one of the current source transistors to operate in the triode region to reduce the minimum amount of voltage that must be allocated to that device. They achieved a modest increase in signal swing at the expense of a decrease in the dc gain but the technique does not appear to offer much potential for more substantial reductions in supply voltage.

Although the negative output impedance compensation technique has been around for quite a while [4][11][22][23][24][25], it has received little attention. This gain enhancement technique is also termed positive feedback gain enhancement technique because it applies positive feedback to generate a compensating negative conductance for the purpose of enhancing the amplifier gain. In the context of very low voltage circuits, however, this technique offers potential for overcoming some of the fundamental limitations that are inherent in the other more popular gain enhancement approaches. The negative output impedance gain enhancement technique has potential for achieving very high

gains even with serious MOS drain conductance degradation and it does offer potential for energy-efficient fast settling in low voltage precesses.

The first trust in this research is focused on the design of high gain fast-settling operational amplifiers with a new negative conductance DC gain enhancement technique suitable for low voltage processes.

1.1.2 Fast-settling amplifiers

In many applications of op amps, the settling time of the amplifiers directly determines the system performance. For example, the limited settling time of the inter-stage amplifiers is one of the major obstacles limiting high sampling rates in high resolution pipelined ADCs. Fast-settling translates, in part, to the requirement of a large GBW of the op amp. The technique that has been proposed to improve bandwidth uses a high frequency feedforward path [26][27]. Generally, feedforward is used to bypass an amplifier or level translator stage that has a poor high-frequency response. Feedforward compensation techniques have also been used to stabilize operational amplifiers in low voltage applications [28][29][30]. The conventional feedforward techniques use an ac bypass capacitor as the feedforward element connecting the input to the output or to intermediate output nodes. One undesirable property inherent in many feedforward compensation schemes is the existence of slow-settling components in the step response of the amplifier. This is caused by imperfect pole-zero cancellation [31]. Although large feedforward capacitors will reduce the mismatch between the pole-zero pairs, if the capacitance values become too large the response time will degrade due to slew rate limitations. A new feedforward compensation method was proposed in [32] to stabilize feedback amplifiers. With a simple feedforward amplifier, the bandwidth of the stabilized amplifier is close to its uncompensated bandwidth. In [33], two new circuit techniques to broad-band the GBW of CMOS folded-cascode amplifiers were presented. Although these

feedforward techniques offer the advantage of higher pole zero cancellation frequencies, the exact pole-zero cancellation is affected by the parasitic capacitances.

The second trust in this research work is focused on developing a new feedforward compensation amplifier structure which can boost the bandwidth of amplifiers. The feedforward signal path introduces zeros in the open-loop transfer function that are used to shape the overall frequency response by using the zeros for pole-zero cancellation. Formulas are derived for exact pole-zero cancellation. As a result, the unity-gain frequency of the amplifier can be extended and the slow-settling components inherent in many feedforward compensation schemes can be reduced.

1.2 An Asynchronous Delay-Line Based Data Recovery/ Retransmission System and Characteristics of Delay Cells

Most existing commercial high speed serial data recovery techniques are based on using a local voltage controlled oscillator (VCO) and a phase-locked loop (PLL) [34][35] to generate a recovered clock which is used to sample the incoming data [36][37][38][39]. Two fundamental limitations of such PLL-based data recovery systems are the long acquisition time required for locking onto the incoming data and the susceptibility to jitter on the incoming data. A new technique for asynchronous data recovery based upon using a delay line in the incoming data path is introduced. The proposed asynchronous delay-locked loop (DLL) based approach for serial data recovery and retransmission uses no clock to sample the incoming data sequence. It samples incoming data in the voltage controlled delay line (VCDL) on transitions of the data itself. The proposed data system has a reduced sensitivity to jitter on incoming data when compared to standard PLL-based data recovery systems. It actually recovers all data in the channel for a fixed interval prior to the first data transition. Two key performance characteristics must be satisfied for successful operation of this system. First, the delay T of the delay line must be close to the period of the data clock Td. Second, the delays in

each stage must be equal and independent of the input data sequence. Several delay cell structures are investigated. A data independent delay cell required in the proposed data recovery system is introduced.

1.3 Dissertation Organization

This dissertation consists of seven chapters. The main emphasis of the work is on the development of a design strategy for enhancing the DC gain and settling performance of amplifiers which are suitable for low-voltage operation. The research motivations for the three trusts of this research are discussed in Chapter 1. In Chapter 2, open-loop pole bounds for positive feedback operational amplifiers are derived. It provides circuit designers with stability guidelines for positive feedback amplifier design. A new negative conductance voltage gain enhancement technique is introduced in Chapter 3. A fully differential high gain amplifier is designed based on the proposed gain enhancement technique. A prototype operational amplifier was fabricated in the AMI 0.5um CMOS process to validate the fundamental performance characteristics of the negative conductance gain enhancement technique. Experimental results for the high gain amplifier with negative conductance gain enhancement are presented in Chapter 4. A new fast-settling amplifier structure with bandpass feedforward compensation is presented in Chapter 5. In Chapter 6, an asynchronous delay-Line based data recovery /retransmission system is introduced. Several delay cell structures are investigated. A data independent delay cell required in the proposed data recovery system is introduced. Conclusions are given in Chapter 7.

CHAPTER 2. STABILITY AND METASTABILITY ISSUES OF NEGATIVE CONDUCTANCE VOLTAGE GAIN ENHANCEMENT TECHNIQUE

2.1 Introduction

CMOS technology scaling has enabled dramatic increases in integrated circuit performance over the years. As the device sizes become smaller, the result has been an increase in the number of transistors and functions per chip, improvements in circuit speed, and a reduction in the power consumed per transistor. For digital circuits there have been increases in performance through device scaling. As device dimensions shrink, the parasitic capacitances tend to decrease. Furthermore, the reduction in channel length and gate oxide increase the current density, achieving more current drive in the same area. This enables faster charging and discharging of the load capacitance and lower propagation delays. Higher throughout and higher clock rates can be achieved for digital circuits. On the other hand, the voltage supply needs to be scaled down with device dimensions due to the demand for low-power circuit, and the unavoidable issue of dielectric breakdown in devices with thinner gate oxides. The popularity of portable applications, such as cellular phones and labtop computers has created a strong demand for low-power IC circuits. The power in digital circuits is a strong function of the supply voltage with lower supply voltages resulting in a reduction of the power consumption. It is clear that the operating voltage for CMOS technology will be at 1.5V and below throughout the remainder of this decade [40]. For mixed-signal applications, the reduction in supply voltage presents new challenges. With supply voltages of 1.5 V and lower, new technology-independent circuit techniques need to be developed.

As the supply voltage is scaled down, the voltage available to represent the signal is reduced. This introduces several factors that complicate of the design of low-voltage analog circuits.

Specifically, for high gain op amp design, conventional gain enhancement techniques such as cascoding are not viable. As discussed in Chapter 1, the negative conductance voltage gain enhancement technique offers potential for overcoming some of the major obstacles that are inherent in the other more popular gain enhancement approaches. It has potential for achieving very high gains for low voltage operation even with serious MOS drain conductance degradation and it does offer potential for energy-efficient fast settling. This chapter will focus on the negative conductance voltage gain enhancement technique.

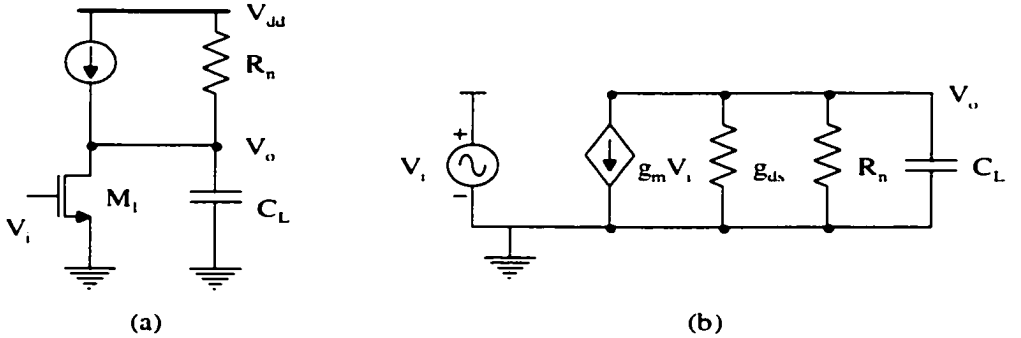
2.2 Basic Concept of the Negative Conductance Gain Enhancement Technique

The basic well-known concept of gain enhancement by negative impedance compensation is shown in Figure 1a. The resistor R_n which is ideally negative, is placed in parallel with the output impedance of the basic amplifier and the total capacitance C_L at the output node V_o. It follows from the small signal equivalent circuit shown in Figure 1b that the voltage gain of the amplifier is

$$A_V(s) = \frac{v_o}{v_i} = \frac{-g_m}{sC_L + g_o^*} \tag{1}$$

where

$$g_o^* = g_{ds} + \frac{1}{R_n} \tag{2}$$



(a) (b)

Figure 1. Basic concept of gain enhancement by negative resistance (a) amplifier stage (b) small signal equivalent circuit

The DC gain of the amplifier is given by the expression

$$A_0 = \frac{-g_{m1}}{g_o^{\bullet}} \tag{3}$$

The amplifier has an open-loop pole p at

$$p = \frac{-g_o^{\bullet}}{C_L} \tag{4}$$

From the DC gain expression (3) it is apparent that the magnitude of DC gain becomes very large, or theoretically infinite as the resistance R_n becomes negative and makes $g_o^{\bullet}$ very small or close to zero. From the open-loop pole p expression (4), it is observed that as R_n is decreased, the open-loop pole crosses into the right half-plane when $1/R_n = -g_{ds1}$.

The characteristics of the amplifier with negative conductance enhancement can be summarized as follows.

1. The DC gain can be very large. It can achieve very high gains even with serious MOS drain conductance degradation.
2. The gain enhancement does not require stacked transistors between power supply rails and thus it has the potential for operating at very low voltages.
3. The gain enhancement approach does not introduce additional internal nodes and thus it does not adversely reduce the high-frequency response of the basic amplifier so wide bandwidth can be realized.
4. The amplifier may have right-half plane open loop poles.

Although the negative output impedance compensation technique has been around for quite a while [4][11][25], it has received little attention. For conventional op amp design, op amp open loop poles are in the left-half plane. For amplifiers with negative impedance gain enhancement the open

loop pole can cross from the left half-plane into the right half-plane as the negative resistance R_n changes in value. There are three major concerns that limit the widespread adoption of this gain enhancement technique. The first concern is the stability of the feedback amplifier if the op amp has a right-half plane open-loop pole. The second concern is the metastability of the amplifier if it has a right-half plane open-loop pole. The third concern is the practicality of achieving high DC gain. We will discuss stability and metastability issues of the negative gain enhancement technique in this chapter and discuss the practicality issue in next chapter.

2.3 Existing Scheme Perceptions

Generally, a compensating negative conductance is generated by applying positive feedback from the output node. The most common negative conductance gain enhancement technique is based upon what is called $-g_m$ compensation achieved by cross-coupling a pair of load devices on the standard differential pair. One typical implementation of the negative conductance discussed by Allstot [11] is shown in Figure 2. It uses a cross-drain-coupled differential pair to generate the

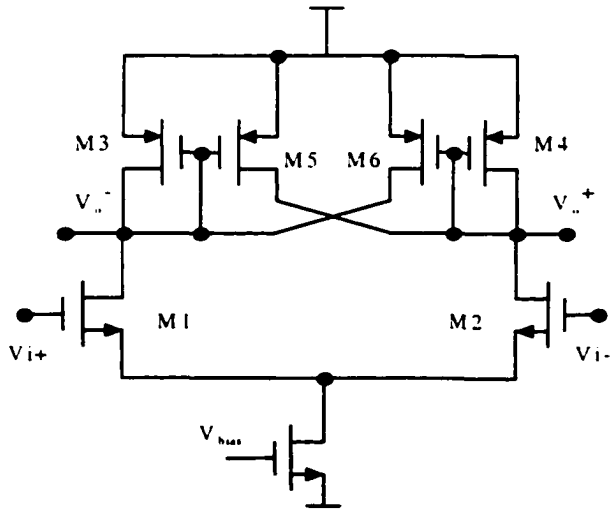


Figure 2. Implementation of negative impedance by cross-drain-coupled differential pair

conductance. Assuming the circuit is symmetrical and matched, a small signal analysis of this circuit gives the gain equation

$$A_0 = \frac{V_o^+ - V_o^-}{V_i^+ - V_i^-} = \frac{-g_{m1}}{g_{ds1}+g_{ds3}+g_{ds6}+g_{m3}-g_{m6}} \qquad (5)$$

If $g_{m6} = g_{ds1} + g_{ds3} + g_{ds6} + g_{m3}$, then the amplifier will exhibit an infinite DC gain. To get a very high DC gain we need almost perfect matching between g_{m6} and the sum of $g_{ds1} + g_{ds2} + g_{ds3} + g_{m3}$. Since the transconductance g_m of each transistor is quite sensitive to temperature and process variations, any mismatches between g_{m3} and g_{m6} may cause the gain to vary dramatically or actually cause a gain sign reversal. If the gain reversal occurs, the stage will operate as a cross-coupled latch.

Although the major drawback of this technique is the difficulty in accurately matching $-g_m$ to the sum of g_m and g_{ds} terms over process and temperature variation to achieve DC gain enhancement, some researchers had reported the limitation of this technique is the susceptibility of right-half plane open loop poles. In a resent discussion of this technique, Gregorian [41] suggested that a practical boosting of gain by 3 to 4 was possible to avoid a $-g_m$ compensated amplifier with a right-half plane, (RHP) op amp pole. Wang and Harjani [42] suggested more stringent requirements of this gain enhancement technique in order to avoid the right-half plane op amp pole. According to their 6σ criterion, they suggested that the maximum practical gain enhancement could be 3.5 for a reasonable yield. Their conclusions were consistent with those of Gregorian's. Actually, Laber and Gray [4] had previously observed that the right-half plane open-loop pole is generally not of major concern since feedback will generally move the closed-loop pole into the left half-plane. When designing amplifiers with the negative impedance gain enhancement technique, amplifiers should be designed to meet closed-loop pole, not LHP open-loop pole bounds.

Some researchers had expressed concern about the meta-stability problem. When the amplifier has a right-half plane open loop pole it will have meta-stability problem for open loop configuration. Since most high gain amplifiers are used in a close loop configurations, as long as the external network provides enough negative dc feedback and moves the closed loop poles into the left-half plane, meta-stability will not be a concern.

Open loop pole location bounds for positive feedback gain enhancement operational amplifiers will be derived in the next section. We will also show the closed-loop system is generally not affected by meta-stability concerns.

2.4 Open Loop Pole Location Bounds for Positive Feedback Gain Enhancement Operational Amplifiers

Consider the standard feedback amplifier shown in Figure 3. If the feedback ratio is β, the closed loop transfer function can be written as equation (6)

$$A_f(s) = \frac{V_{out}}{V_i} = \frac{A(s)}{1 + \beta A(s)} \tag{6}$$

where A(s) denotes the transfer function of an amplifier with negative impedance compensation.

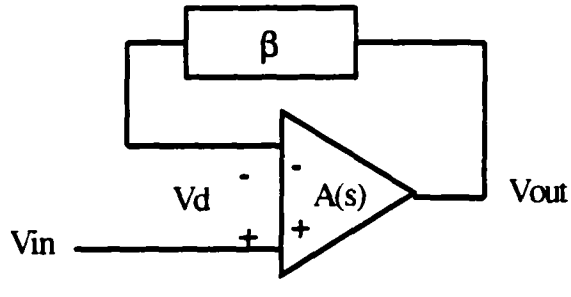


Figure 3. Signal flow graph for closed-loop configuration

Assuming the operational amplifier is a first-order system, its open loop transfer function can be expressed as

$$A(s) = \frac{V_{out}}{V_d} = \frac{A_0}{\frac{s}{p} - 1} = \frac{A_0 p}{s - p} \tag{7}$$

where A_0 is the DC gain and p is the open-loop pole of the amplifier. If the op amp is based on the structure shown in Figure 1, the DC gain will have the form of $A_0 = g_m/g_o^*$ and the open-loop pole p will have the form of g_o^*/C_L. The open loop pole p is adjustable and it can be in the left-half plane or in the right-half plane. If $g_o^* < 0$, the amplifier has an open loop pole in the left-half plane; If $g_o^* > 0$, the amplifier has an open loop pole in the right-half plane. The product of A_0 and p is the gain-bandwidth product of the amplifier and is denoted as GB. Note that for the structure of Figure 1, GB is a positive constant and is independent of the pole location p. The open loop transfer function A(s) can be rewritten as

$$A(s) = \frac{GB}{s - p} \tag{8}$$

Substituting (8) into (6) we obtain the feedback amplifier transfer function

$$A_f(s) = \frac{GB}{s - p + \beta GB} \tag{9}$$

It is apparent that the closed-loop p_f can be expressed as

$$p_f = p - \beta GB \tag{10}$$

The stability of the closed-loop amplifier will be determined by the location of the closed-loop pole p_f. p_f will be derived for different open-loop pole locations as follows.

Case 1. A(s) has a LHP pole, i.e., $p < 0$

Since $A_0 < 0$ and $\beta GB > 0$, it follows that $p_f < 0$

Thus the open loop amplifier is stable and the closed-loop amplifier is also stable.

Case 2. A(s) has a RHP pole, i.e., $p > 0$

Since $A_0>0$ and $\beta GB > 0$, it follows from (10) that

$p_f < 0$ if $0< p < \beta GB$ and $p_f > 0$ if $p > \beta GB$

Thus the open loop amplifier is unstable while the close loop amplifier is stable if $0< p < \beta GB$.

Therefore, closed-loop pole stability bound is

$$p < \beta GB \tag{11}$$

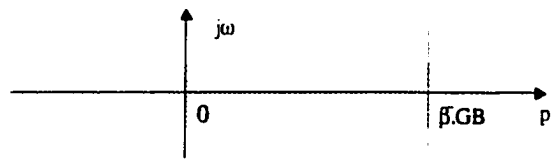
The closed-loop stability bounds are depicted in Figure 4. From this figure, it is apparent that there is a wide range for stable closed-loop amplifiers even if the open-loop amplifier is unstable.

According to equation (8), the open loop DC gain is

$$A(j0) = -\frac{GB}{p} \tag{12}$$

According to equation (9), the closed loop DC gain is

$$A_f(j0) = \frac{GB}{-p + \beta GB} \tag{13}$$



•Stable open loop amplifier	•Unstable open loop amplifier	•Unstable open loop amplifier
•Stable closed-loop amplifier	•Stable closed-loop amplifier	•Unstable closed-loop amplifier

Figure 4. Closed-loop pole stability bound $p<\beta GB$

The open loop DC gain versus the open loop pole location p is plotted in Figure 5a. Note the DC gain of A(s) is asymptotic to $+\infty$ from the left of the origin and asymptotic to $-\infty$ from the right of the origin. Around p=0, the magnitude of open loop DC gain is very high irrespective of whether the open-loop pole is in the right or the left half-plane. The pole frequencies p_{min} and p_{max} will be discussed later. The closed-loop gain versus p is shown in Figure 5b. As expected, the closed loop gain is exactly $1/\beta$ when the open loop pole is at the origin. It approaches $+\infty$ as p approaches βGB from the left and approaches $-\infty$ as p approaches βGB from the right. Of course, the feedback amplifier will be unstable if $p>\beta GB$. The region of interest of $A_f(j0)$, however, is far from the closed-loop pole stability bound βGB and is ideally in the vicinity of p=0 so that the closed-loop amplifier is guaranteed to be stable.

As indicated before, conventional wisdom suggests only modest gain-boosting is achievable because of concern about RHP open-loop poles. It can be shown that RHP open-loop pole amplifiers can actually improve settling performance of closed-loop amplifiers.

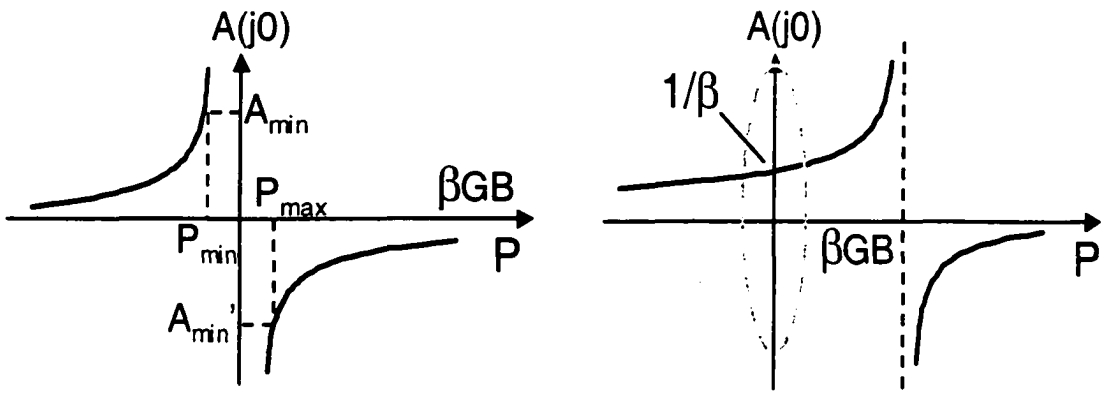


Figure 5. Operation of positive feedback amplifier (a) open-loop DC gain, (b) closed-loop DC gain

Existing approaches to amplifier design in which the open loop amplifier is stable have a unit step response shown in Figure 6. The settling time t_s is defined as the time required to settle within the settling windows which are depicted by the $(1+\varepsilon)$ and the $(1-\varepsilon)$ bounds around the desired value of $1/\beta$ where ε is the settling accuracy and is determined by application requirements. The actual amplifier settling asymptote; $1/\beta\ (1-\varepsilon_1)$, differs from $1/\beta$ because of a non-infinite open loop DC gain of the op amp.

For example, in a 10-bit application, if the entire error budget is allocated to the settling of the amplifier, then $\varepsilon \approx 0.001$ and the corresponding DC open loop gain requirement of the amplifier for $\beta=1$ must be somewhat over 1000 to achieve this value of ε_1. To meet this requirement, ε_1 must be smaller than ε and this further increases the open-loop gain requirements of the amplifier. Corresponding to each ε_1 is a DC gain requirement for the operational amplifier.

If we now return to the pole-adjustable amplifier characterized by equation (7), it is apparent that the DC gain can become very large as p approaches the origin. This causes the $1/\beta\ (1-\varepsilon_1)$ asymptote of Figure 6 to move up and as the open loop amplifier gain goes to ∞, the asymptote

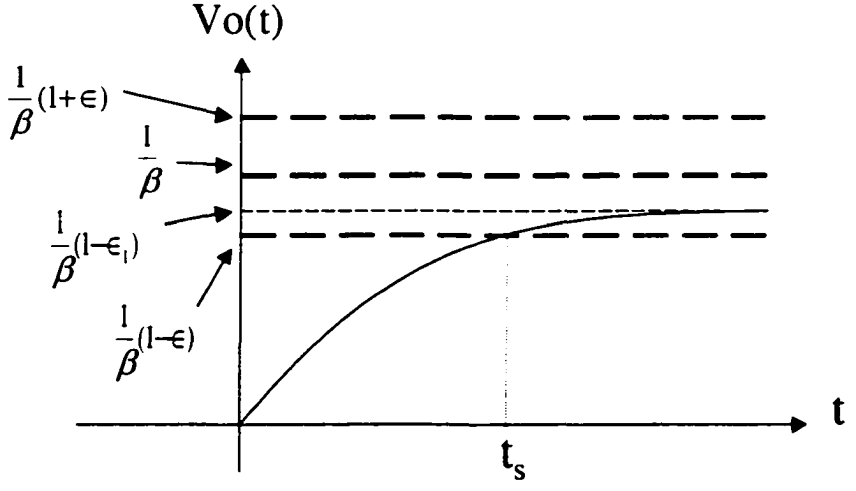


Figure 6. Unit step response of conventional amplifier

becomes 1/β and actually moves above 1/β as the open loop pole moves into the right-half plane. If we move the open loop pole too far into the right-half plane, the settled value will go outside of the acceptable value around 1/β. With these observations, the gain bounds and correspondingly the pole bounds can be determined for the pole-adjustable amplifier to have a pre-determined asymptote. Consider an expansion of Figure 5b around the region of interest-specifically around p=0. This is shown in Figure 7.

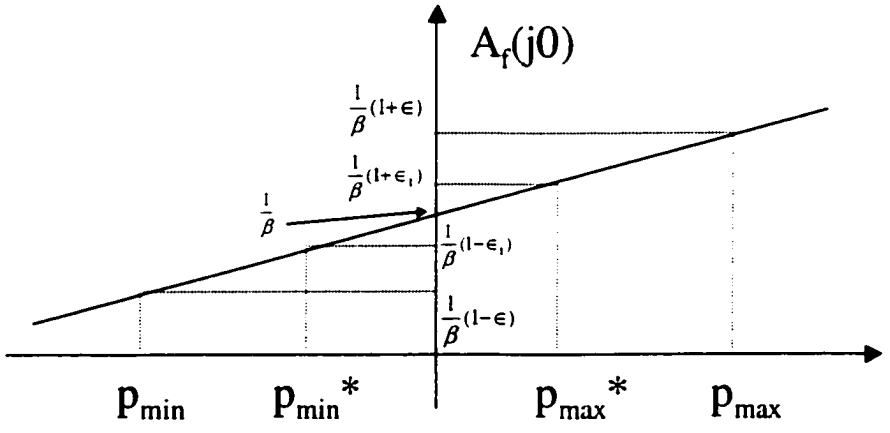


Figure 7. Expansion of the Figure5 b around the origin

Mathematically, the closed-loop gain bounds must satisfy the inequality

$$\frac{1}{\beta}(1-\varepsilon) < A_f(j0) < \frac{1}{\beta}(1+\varepsilon) \tag{14}$$

This is equivalent to the inequality for open loop pole p

$$-\frac{\varepsilon\beta GB}{1-\varepsilon} < p < \frac{\varepsilon\beta GB}{1+\varepsilon} \tag{15}$$

The pole bounds for a given settling accuracy requirement are

$$P_{min} = -\frac{\varepsilon\beta GB}{1-\varepsilon} \tag{16}$$

$$P_{max} = \frac{\varepsilon\beta GB}{1+\varepsilon} \tag{17}$$

Inequality (15) establishes the second open-loop pole bound for positive feedback gain enhancement amplifiers. This bound is the settling requirement pole bound.

Actually, amplifiers should be designed to settle within the settling windows $1/\beta(1\pm\varepsilon_1)$ to meet the settling accuracy requirement ε. Therefore the closed-loop DC gain should be satisfy to meet the inequality

$$\frac{1}{\beta}(1-\varepsilon_1) < A_f(j0) < \frac{1}{\beta}(1+\varepsilon_1) \tag{18}$$

This is equivalent to the inequality for open loop pole p

$$-\frac{\varepsilon_1\beta GB}{1-\varepsilon_1} < p < \frac{\varepsilon_1\beta GB}{1+\varepsilon_1} \tag{19}$$

The pole bounds are

$$P_{min}^{\cdot} = -\frac{\varepsilon_1\beta GB}{1-\varepsilon_1} \tag{20}$$

$$P_{max}^{\cdot} = \frac{\varepsilon_1\beta GB}{1+\varepsilon_1} \tag{21}$$

Inequality (19) establishes the third open-loop pole bounds for positive feedback gain enhancement amplifiers. These bounds are the amplifier open loop pole design bounds. P_{min}, P_{max}, P_{min}*, and P_{max}* are shown in Figure 7.

As an example, assume a 10-bit accuracy amplifier is to be designed with positive feedback gain enhancement technique. This requires the amplifier must be settled with an ε of 0.1%. Assume β=1, GB=50MHz, and ε_1 =0.05%, Figure 8 shows three open-loop pole bounds. Figure 8 shows that the open loop pole of the amplifier is designed far from the closed-loop stability bound. In such a way, the stability of the open loop amplifier is not a concern.

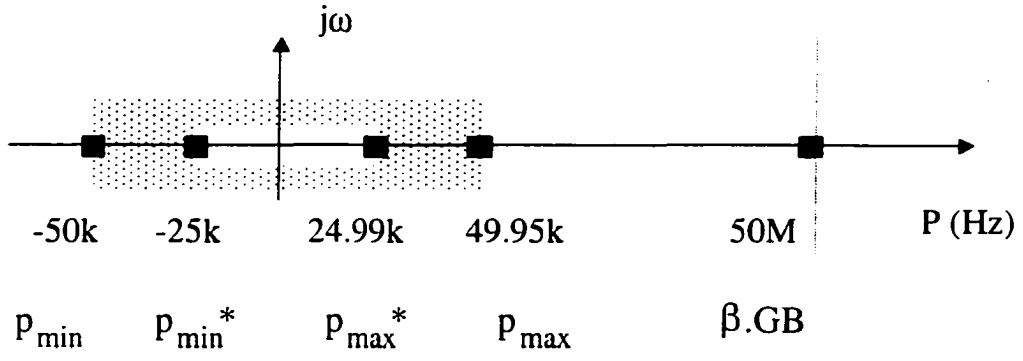
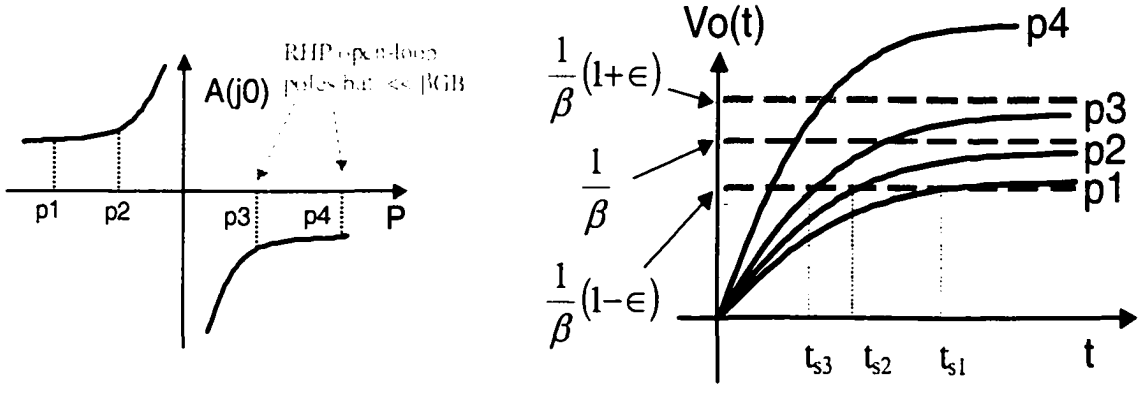


Figure 8. Example of three open-loop pole bounds

For a unity step input, the settling response of the single-pole amplifier is found to be

$$Ts(t) = \frac{GB}{\beta.GB - p}(1 - e^{-(\beta GB - p)t})u(t) \tag{22}$$

For different open-loop pole locations p1-p4 shown in Figure 9a, the corresponding unity step response is shown in Figure 9b. These plots not only show that the amplifier is stable when the open-loop pole is modestly in the right half-plane but it also exhibits both faster and more accurate settling when the open-loop pole is moved slightly into the RHP.



(a) (b)

Figure 9. (a) Open loop pole location (b) step responses

2.5 Meta-Stability

2.5.1 Open loop DC transfer function

Figure 10 conceptually illustrates the DC transfer characteristics for operational amplifiers with negative impedance gain enhancement. These transfer curves show the effects of increasing the negative conductance (from curve 1 to curve 3). Curve 1 represents the case where the amplifier has a LHP open-loop pole. The total effective output conductance is positive thus the DC gain of the amplifier is only slightly enhanced. Curve 2 represents the case where the amplifier output conductance cancellation becomes more completed. The total effective output conductance is a very small positive value thus the DC gain of the amplifier is greatly enhanced and the open-loop pole is slightly in the LHP. Curve 3 represents the case where the total output conductance is negative. In this case the amplifier has a RHP open loop pole. For curve 3, there is an 180° phase shift in the high gain region between V_{imin} and V_{imax} we term this phase reversal.

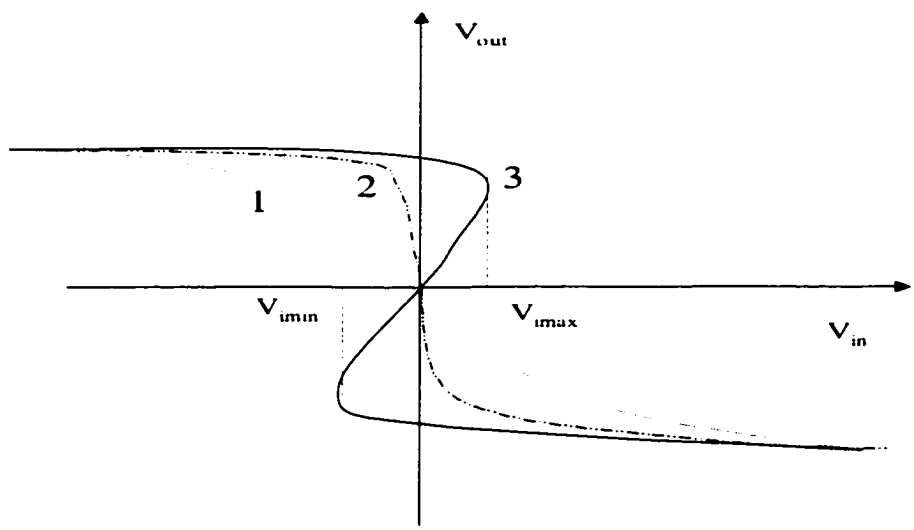


Figure 10. DC transfer function

2.5.2 Open loop amplifier meta-stability

For curve 1 and 2, each input operating point corresponds to only one output operating point. On the other hand, for curve 3 there is a range of input operating points that each corresponds to three output operating points. The input range for this multi-values output is between V_{imin} and V_{imax}. This defines a state of unstable equilibrium (also known as a meta-stable state). In the metastability region, any disturbance, such as that caused by noise, causes the amplifier to switch to one of its three stable states. Therefore, RHP open-loop pole operational amplifiers will have meta-stability problems in open loop applications. However, if RHP open-loop pole amplifiers are used in practical negative feedback configuration, closed loop amplifiers will not suffer meta-stability problems. The closed-loop metastability issue is discussed in the following section.

2.5.3 Closed loop amplifier meta-stability

Let's consider the circuit shown in Figure 11, which consists of one op amp with gain A(s) and two equal-valued resistors R. Assume A(s) is a differential in single-ended out amplifier with a DC gain of A_0 and a RHP open-loop pole. Thus A(s) will have an open loop DC transfer characteristic similar to curve 3 shown in Figure 10.

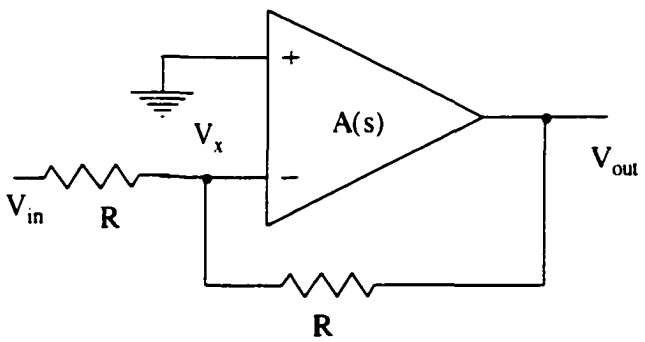


Figure 11. Single-ended closed loop amplifier

Assume the voltage at the inverting terminal of the op amp is V_x. Since the positive input terminal is grounded, the voltage at the negative terminal must be $-V_{out}/A_0$. Applying KCL at the inverting input node, we obtain the expression

$$\frac{V_{in}-V_x}{R}=\frac{V_x-V_{out}}{R} \tag{23}$$

The output voltage V_{out} can thus be determined as

$$V_{out}=2V_x-V_{in} \tag{24}$$

Equation (24) indicates that each closed loop input V_{in} only corresponds to one output operating voltage V_{out} thus the metastability problem does not exist in the closed loop amplifier. The closed-loop metastability characteristics are superimposed on the open-loop transfer characteristics in Figure 12 and a family of closed-loop lines corresponding to (24) show only a single intersection with the open-loop transfer characteristics for each value of V_{in}. Although the locus of (24) was derived for a feedback factor β of ½ in Figure 11, a single intersection point will be obtained for all V_{in} for all practical feedback factors. It can thus be concluded that the meta-stability problems do not exist in the closed-loop amplifier.

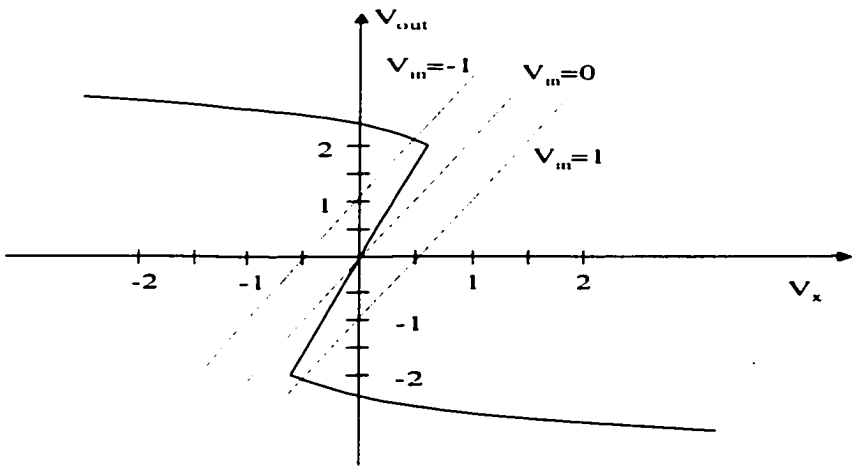


Figure 12. The closed loop amplifier does not have a metastable state

2.6 Conclusion

Two important properties of amplifiers with negative impedance gain enhancement were discussed in this chapter. The first property is stability. Incorrect existing wrong perceptions regarding stability of positive feedback amplifiers were pointed out. Three open loop pole bounds were derived to ensure stability and settling performance of amplifiers with negative impedance gain enhancement. Amplifiers should be designed to meet actual open loop pole bounds, not LHP pole bound. The second property discussed is the meta-stability issue. Although open loop amplifiers may have meta-stable states, practical closed loop amplifiers will not have such states indicating meta-stability is not of concern in the feedback amplifiers.

CHAPTER 3. NEW NEGATIVE CONDUCTANCE VOLTAGE GAIN ENHANCEMENT TECHNIQUE

3.1 Problems of Existing Circuit Implementations of the Negative Impedance Gain Enhancement Technique

As discussed in Chapter 2, several circuit implementations of amplifiers with the negative impedance gain enhancement technique have been reported. To get a very high DC gain, very close matching between the positive output impedance and the negative compensated conductance is required to achieve the required conductance cancellation. For the negative impedance gain enhancement technique, the key concern is how practically the circuit can meet the matching requirement.

As discussed in Chapter 2, the most common negative conductance gain enhancement technique is based upon what is called –gm compensation which is achieved by cross-coupling a pair of load devices on the standard differential pair. One implementation of the negative impedance discussed by Allstot is shown in Figure 2 [11]. It uses a cross-drain-coupled differential pair to generate the negative impedance. The gain equation for that circuit is

$$A_d=\frac{V_o^+-V_o^-}{V_i^+-V_i^-}=\frac{-g_{m1}}{g_{ds1}+g_{ds3}+g_{ds6}+g_{m3}-g_{m6}} \tag{25}$$

Although it may appear from (25) that the major challenge for this gain enhancement technique requires matching of two transconductances, the larger challenge is actually to match a negative transconductance to the sum of a transconductance and several output conductance terms. Wang and Harjani [42] discussed the design of amplifiers with this –gm compensation gain enhancement technique. They demonstrated a simulated DC gain close 60 dB. Szczepanski et al also

used similar cross-coupled transistors to generate a negative transconductance [43]. They showed a SPICE simulated DC gain of 50dB.

Nauta applied negative resistance to a simple inverter transconductor in order to increase the DC gain of the transconductor [22][23]. In the Nauta circuit, the negative resistance is generated by applying differential output signals to matched inverters. The negative resistance is proportional to $1/\Delta g_m$. A DC gain of 46dB with a 10V power supply was reported. In Wong and Salama's implementation [25], positive feedback was applied to generate an effective negative load conductance which is given by g_m*A+g_{ds}, where A denotes the amount of feedback applied to the gate. Although a gain of 80dB was reported in [25] with a 10V power supply voltage, the gain-bandwidth-product was only 12MHz for a 5pF capacitor load. The structure in [25] requires a high frequency, high differential gain stage to achieve conductance cancellation. This gain stage introduces internal nodes and thus limits the high-frequency response of the amplifier. Laber and Gray [4] described a CMOS folded cascoded operational transconductance amplifier that achieved high DC gain by using an internal positive feedback loop. The positive feedback loop generates a negative conductance which is used to compensate a positive conductance plus a positive transconductance. If the negative conductance perfectly matches the positive conductance, the overall DC gain becomes the quad of the intrinsic MOS transistor gain g_m*r_o. If a mismatch between the negative conductance and the positive conductance exists, the overall DC gain is proportional to $(g_m*r_o)^2(roc/\Delta roc)$. They reported a DC gain over 100dB but this is mainly due to the cascoded structure used and at the expense of output swing.

Almost all existing amplifier structures share a common characteristic, a negative transconductance is used to compensate for positive output conductances and/or transconductances. In these approaches, achieving large gain enhancement requires the precise negative transconductance

compensation for the positive output conductance. The major drawback of using negative transconductance $-g_m$ to compensate for the output conductance g_{ds} is the inability to accurately match these terms because g_m is usually much larger than g_{ds} making large gain enhancement difficult to achieve. Also, both g_m and g_{ds} are sensitive to bias current, process and temperature but in much different ways [24]. Therefore, directly using a negative g_m to compensate for the positive output conductance g_{ds} offers little potential for practical applications when very high dc gains are required.

The matching requirement can be relaxed by making one of the important parameters programmable. For example, one way to maintain the very high DC gain can be achieved by making the negative compensated conductance adjustable to track the change of the positive output impedance due to process and/or temperature variations. None of the existing amplifier schemes discussed and/or showed gain control ability.

3.2 Proposed Negative Conductance Gain Enhancement Technique

A basic amplifier is shown in Figure 13a. The low frequency voltage gain is given by

$$A_0 = \frac{-g_{m1}}{g_{ds1} + g_{ds2}} \tag{26}$$

A new negative conductance gain enhancement scheme [44] is shown conceptually in Figure 13b. A PMOS transistor M_c is placed at the output of the basic amplifier. A low gain stage A is connected between the drain and the source of M_c. Transistor M_c is biased in the saturation region and its gate-source voltage is AC shorted. Body effects can be ignored if an n-well CMOS process is used and the bulk terminal of M_c is tied to its source. If the gain of the low gain stage A is larger than 1, then a negative conductance of $(A-1).g_{dsc}$ will be presented in parallel with the output of the basic amplifier.

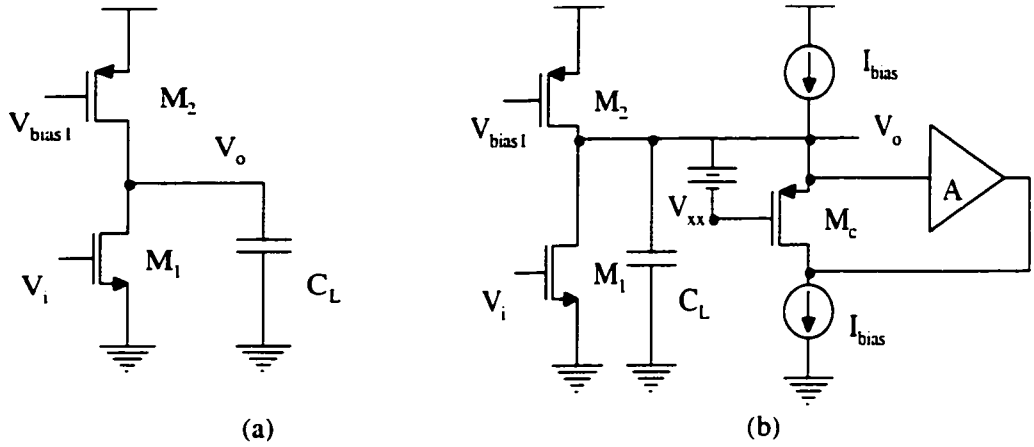


Figure 13. (a) Basic amplifier (b) Proposed negative conductance gain enhancement scheme.

Assume the capacitance at the output node is C_L. This circuit has a transfer function given by the expression

$$A(s)=\frac{-g_{m1}}{sC_L+g_{ds1}+g_{ds2}+g_{dsc}(1-A)} \tag{27}$$

The DC gain is

$$A_0=\frac{-g_{m1}}{g_{ds1}+g_{ds2}+g_{dsc}(1-A)} \tag{28}$$

If $g_{ds1}+g_{ds2}=(A-1)g_{dsc}$, the DC gain of the amplifier will be infinite.

The proposed circuit generates a negative conductance that is only function of g_{ds} and is not related to g_m. Therefore, a negative g_{ds} can realistically match positive g_{ds} terms and the matching requirements for achieving very high DC gain are less stringent than for the existing $-g_m$ gain enhancement schemes. Further, this circuit has the potential for precise digital control of a large dc gain by exploiting the property that there is a phase reversal as the pole crosses the origin in the open-

loop transfer function and this phase reversal can be detected. Since $g_{ds}=\lambda I_{DQ}$, the negative conductance is easily adjustable through the adjustment of the biasing current of transistor M_c.

3.3 DC Gain Sensitivity

For the negative impedance gain enhancement technique, gain enhancement requires the precise negative conductance compensation for the positive output conductance. Existing negative transconductance gain enhancement techniques generate a negative transconductance while the proposed negative conductance gain enhancement technique generates a negative conductance. Since both g_m and g_{ds} are sensitive to process and temperature, the DC gain of the op amp is sensitive to process and temperature. The sensitivity of the DC gain for the process variation can be modeled with process-related parameters such as threshold voltages V_{tn} and V_{tp} and channel modulation parameter λ. The sensitivities of the DC gain due to process-induced deviations are discussed in this section. The sensitivity of the DC gain due to temperature-induced deviations for the proposed negative conductance voltage gain enhancement technique will be discussed in Section 3.4.

Assuming the DC gain is termed Ad. The DC gain sensitivity due to deviations in variable γ is defined as

$$S_{\gamma}^{Ad} = \frac{\partial A_d}{\partial \gamma}\frac{1}{A_d} \tag{29}$$

First let's consider the amplifier with conventional negative transconductance gain enhancement shown in Figure 2. The DC gain can be expressed with DC operating point parameters and process parameters as follow:

$$A_{d1} = \frac{g_{m1}}{g_{ds1} + g_{ds3} + g_{ds6} + g_{m3} - g_{m6}}$$

$$= \frac{\mu_n C_{ox}(W/L)_1(V_{gs1} - V_{tn})}{(\lambda_n + \lambda_p)\frac{\mu_n C_{ox}(W/L)_1(V_{gs1} - V_{tn})^2}{2} + \mu_p C_{ox}(V_{gs3} - V_{tp})[(W/L)_3 - (W/L)_6]} \tag{30}$$

For A_{d1} to be large,

$$\frac{\mu_p}{\mu_n}\frac{[(W/L)_3 - (W/L)_6]}{(W/L)_1}\frac{(V_{gs3} - V_{tp})}{(V_{gs1} - V_{tn})^2} \approx -\frac{(\lambda_n + \lambda_p)}{2} \tag{31}$$

The DC gain sensitivity due to deviations in V_{tp} for the negative transconductance gain enhancement amplifier can be derived by substituting equation (30) in equation (29) if we consider only the variable V_{tp}.

$$S_{V_{tp}}^{Ad1} = \frac{\partial A_{d1}}{\partial V_{tp}}\frac{1}{A_{d1}} = A_{d1nom}\frac{\mu_p}{\mu_n}\frac{[(W/L)_3 - (W/L)_6]}{(W/L)_1}\frac{1}{(V_{gs1} - V_{tn})} \tag{32}$$

where A_{d1nom} is the nominal value of the DC gain.

Equation (32) can be simplified if we assume equation (31) is valid.

$$S_{V_{tp}}^{Ad1} \approx -A_{d1nom}\frac{(\lambda_n + \lambda_p)}{2}\frac{(V_{gs1} - V_{tn})}{(V_{gs3} - V_{tp})} \tag{33}$$

Similarly, the DC gain sensitivity due to deviations in V_{tn} can be obtained if we consider only the variable V_{tn}.

$$S_{V_{tn}}^{Ad1} = \frac{\partial A_{d1}}{\partial V_{tn}}\frac{1}{A_{d1}} = A_{d1nom}[(\lambda_n + \lambda_p)(\frac{1}{(V_{gs1} - V_{tn})} - \frac{1}{2}) - \frac{\mu_p}{\mu_n}\frac{[(W/L)_3 - (W/L)_6]}{(W/L)_1}\frac{(V_{gs3} - V_{tp})}{(V_{gs1} - V_{tn})^2}] \tag{34}$$

where A_{d1nom} is the nominal value of the DC gain A_{d1}.

Equation (34) can be simplified if we assume equation (31) is valid.

$$S_{V_{in}}^{A_{d1}} \approx A_{d1nom}(\lambda_n + \lambda_p)\frac{1}{(V_{gs1} - V_{in})} \tag{35}$$

The DC gain sensitivity due to deviations in channel modulation parameter λ_n can be obtained if we consider only the variable λ_n.

$$S_{\lambda_n}^{A_{d1}} = \frac{\partial A_{d1}}{\partial \lambda_n}\frac{1}{A_{d1}} = -A_{d1nom}\frac{(V_{gs1} - V_{in})}{2} \tag{36}$$

The DC gain sensitivity due to deviations in channel modulation parameter λ_p can be obtained if we consider only the variable λ_p.

$$S_{\lambda_p}^{A_{d1}} = \frac{\partial A_{d1}}{\partial \lambda_p}\frac{1}{A_{d1}} = -A_{d1nom}\frac{(V_{gs1} - V_{in})}{2} \tag{37}$$

Now let's consider the amplifier with proposed negative conductance gain enhancement shown in Figure 13b. The DC gain can be expressed with DC operating point parameters and process parameters as follow:

$$A_{d2} = \frac{g_{m1}}{g_{ds1} + g_{ds2} + (1-A)g_{dsn}}$$

$$= \frac{\mu_n C_{ox}(W/L)_1(V_{gs1} - V_{in})}{(\lambda_n + \lambda_p)\frac{\mu_n C_{ox}(W/L)_1(V_{gs1} - V_{in})^2}{2} + \frac{1-A}{2}\lambda_p \mu_p C_{ox}(W/L)_c(V_{gsn} - V_{tp})^2} \tag{38}$$

For A_{d2} to be large,

$$\frac{1-A}{2}\lambda_p \frac{\mu_p}{\mu_n}\frac{(W/L)_c}{(W/L)_1}\frac{(V_{gsn} - V_{tp})^2}{(V_{gs1} - V_{in})^2} \approx -\frac{(\lambda_n + \lambda_p)}{2} \tag{39}$$

The DC gain sensitivity due to deviations in V_{tp} for the negative conductance gain enhancement amplifier can be derived by substituting equation (38) in equation (29) if we consider only the variable V_{tp}.

$$S_{V_{tp}}^{Ad2} = \frac{\partial A_{d2}}{\partial V_{tp}} \frac{1}{A_{d2}} = A_{d2nom}(1-A)\lambda_p \frac{\mu_p}{\mu_n} \frac{(W/L)_c}{(W/L)_1} \frac{(V_{gsn}-V_{tp})}{(V_{gs1}-V_{tn})} \tag{40}$$

where A_{d2nom} is the nominal value of the DC gain A_{d2}.

Equation (40) can be simplified if we assume equation (39) is valid.

$$S_{V_{tp}}^{Ad2} \approx -A_{d2nom}(\lambda_n + \lambda_p) \frac{(V_{gs1}-V_{tn})}{(V_{gsn}-V_{tp})} \tag{41}$$

Similarly, the DC gain sensitivity due to deviations in V_{tn} can be obtained if we consider only the variable V_{tn}.

$$S_{V_{tn}}^{Ad2} = \frac{\partial A_{d2}}{\partial V_{tn}} \frac{1}{A_{d2}} = A_{d2nom}[(\lambda_n + \lambda_p)(\frac{1}{(V_{gs1}-V_{tn})} - \frac{1}{2}) - \frac{1-A}{2}\lambda_p \frac{\mu_p}{\mu_n} \frac{(W/L)_c}{(W/L)_1} \frac{(V_{gsn}-V_{tp})^2}{(V_{gs1}-V_{tn})^2}] \tag{42}$$

Equation (39) can be simplified if we assume equation (39) is valid.

$$S_{V_{tn}}^{Ad2} \approx A_{d2nom}(\lambda_n + \lambda_p) \frac{1}{(V_{gs1}-V_{tn})} \tag{43}$$

The DC gain sensitivity due to deviations in channel modulation parameter λ_n can be obtained if we consider only the variable λ_n.

$$S_{\lambda_n}^{Ad2} = \frac{\partial A_{d2}}{\partial \lambda_n} \frac{1}{A_{d1}} = -A_{d2nom} \frac{(V_{gs1}-V_{tn})}{2} \tag{44}$$

The DC gain sensitivity due to deviations in channel modulation parameter λ_p can be obtained if we consider only the variable λ_p.

$$S_{\lambda_p}^{A_{d2}} = \frac{\partial A_{d2}}{\partial \lambda_p}\frac{1}{A_{d1}} = -A_{d2nom}\left[\frac{(V_{gs1}-V_{tn})}{2} + \frac{1-A}{2}\frac{\mu_p}{\mu_n}\frac{(W/L)_c}{(W/L)_1}\frac{(V_{gsn}-V_{tp})^2}{(V_{gs1}-V_{tn})}\right] \quad (45)$$

For A_{d2} to be large, equation (45) can be simplified if we assume equation (39) is valid.

$$S_{\lambda_p}^{A_{d2}} \approx -A_{d2nom}\frac{(V_{gs1}-V_{tn})}{2}\frac{\lambda_n}{\lambda_p} \quad (46)$$

Expressions (33)(35)(41)(43) show that proposed negative conductance gain enhancement amplifiers have compatible DC gain sensitivities for the process variation parameters V_{tp} and V_{tn} as those of operational amplifiers with conventional negative transconductance gain enhancement. Expressions (37)(36)(44)(46) show that proposed negative conductance gain enhancement amplifiers have better DC gain sensitivities for the channel modulation parameters as those of operational amplifiers with conventional negative transconductance gain enhancement.

3.4 Prototype Design and Description

A prototype high gain fully differential CMOS operational amplifier was designed, laid out, and fabricated based on the proposed negative conductance voltage gain enhancement technique. The design is summarized in this section, and the results of testing are discussed in Chapter 4.

3.4.1 Design goal

The goal of this design was to demonstrate a high gain CMOS operational amplifier with a DC gain of not less than 80 dB, and to validate the fundamental performance characteristics of the negative conductance gain enhancement technique.

3.4.2 Technology

The prototype was fabricated using the AMI Semiconductor (AMIS) 0.5um AMI_C5N process available through MOSIS. The maximum rated voltage supply is 5V, however, the prototype

was designed for reliable operation at 3V. Three levels of metal interconnect and two layers of poly were used. Capacitors were implemented using poly1 and poly2 layers. The capacitance density of these capacitors was 929 aF/um^2. Resistors were implemented using a poly2 layer inside high resistance implant layer. The nominal sheet resistance of these resistors was 946 ohms/sq. The die was packaged in a DIP 40-pin ceramic package with a 0.310 square inch cavity available through MOSIS.

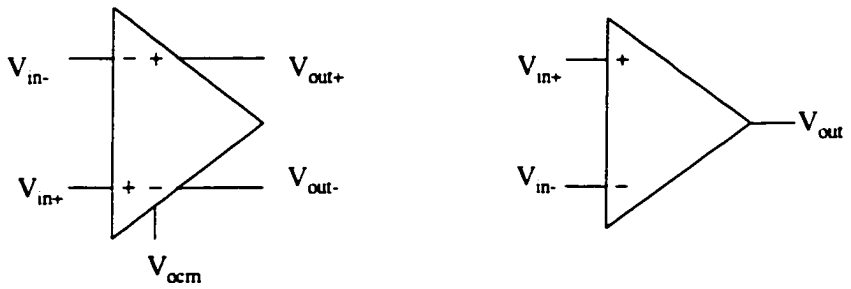
3.4.3 Advantages of fully differential amplifiers

Differential signaling has been widely used in audio, data transmission, and telephone systems for many years because of its inherent tolerance to external noise sources. Today, differential signaling is popular in high-speed data acquisition systems where the ADC's inputs are differential and a differential amplifier is needed to properly drive them [45].

The following characteristics make the use of integrated fully differential amplifiers desirable:

- Tolerant to common mode external noise
- 6-dB increase in dynamic range (ideal for low-voltage systems)
- Reduced second-order harmonics

An integrated, fully differential amplifier is similar in architecture to a standard operational amplifier, with a few differences as illustrated in Figure 14. Both types of amplifiers have differential inputs. Fully differential amplifiers have differential outputs while a standard operational amplifier's output is single-ended. In a fully differential amplifier, the output common-mode voltage can be controlled independently of the differential voltage. The purpose of the V_{ocm} input in the fully differential amplifier is to set the output common-mode voltage. In a standard feedback application of



FULLY-DIFFERENTIAL AMPLIFIER

Differential in

Differential out

Output common-mode voltage set by Vocm

Two feedback paths

STANDARD OPERATIONAL AMPLIFIER

Differential in

Single-ended out

Single feedback path

Figure 14. Fully differential amplifier Vs standard operational amplifier

a single-ended operational amplifier, typically there is one feedback path from the output to the negative op amp input. In a fully differential feedback amplifier, there are generally two identical feedback paths.

3.4.4 Voltage definitions for fully differential amplifier

To understand how a fully differential amplifier behaves, it is important to understand the voltage definitions used to describe the amplifier. The voltage difference between the plus and minus inputs is the input differential voltage, V_{id}. The average of the two input voltages is the input common-mode voltage, V_{ic}. The difference between the voltages at the plus and minus outputs is the output differential voltage, V_{od}. The common-mode output voltage, V_{oc}, is the average of the two output voltages, and is controlled by the voltage at V_{ocm}. These definitions are summarized as

$$V_{id} = V_{in+} - V_{in-} \tag{47}$$

$$V_{ic} = \frac{V_{in+} + V_{in-}}{2} \tag{48}$$

$$V_{od} = V_{out+} - V_{out-} \tag{49}$$

$$V_{oc} = \frac{V_{out+} - V_{out-}}{2} \tag{50}$$

With two inputs and two outputs, there are several voltage gains that can be defined and all, in some applications, are of interest. In many applications, only the ratio between the differential output and the differential input is of concern. Unless specified to the contrary in this dissertation, the term "gain" of the differential input/differential output amplifier will be assured to be defined by the expression

$$A(s) = \frac{V_{od}}{V_{id}} \tag{51}$$

3.4.5 The architecture of the high gain amplifier

A two-stage fully differential high gain amplifier is designed with the proposed negative conductance gain enhancement technique. The block diagram of the amplifier is shown in Figure 15. The amplifier consists of five elements, a basic amplifier, a negative conductance generator (NCG), a common-mode feedback circuit (CMFB), a bias generator, and a second amplifier stage. Details about the two-stage fully differential amplifier are discussed in [46]. For single-stage structures, based upon the proposed negative conductance gain enhancement technique, the resultant feedback amplifier exhibited excellent settling performance for small input steps but my implementations did not achieve the 0.1% settling accuracy level for larger input steps because the dc gain of the amplifier is signal level dependent. Due to the non-linearity of the basic differential stage and the low gain stage in the negative conductance generator, the magnitude of the overall dc gain decreases when a large input step is applied. By adding the second stage, the output signal of the first stage is reduced by a factor of the gain of the second stage. The overall amplifier thus can maintain a large overall voltage gain over a wider output range. In the design discussed in this dissertation, the overall

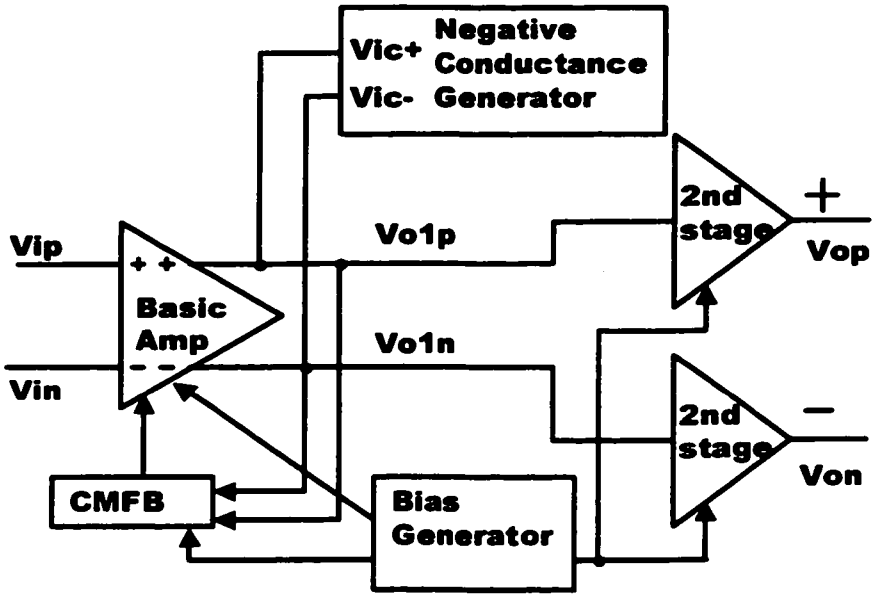


Figure 15. Block diagram of proposed fully differential high gain amplifier

was designed to have most of the dc gain contributed by the first stage while the second stage only provides a gain of 2 to 3. No attempt was made to determine the optimal gain of the second stage.

3.4.6 Transistor-level implementation

A specific transistor-level implementation of the amplifier shown in Figure 15 is described in this section. The basic amplifier is a differential-input, differential-output gain stage. The negative conductance generator is comprised of the low gain stage A, the negative conductance generating transistors and their biasing circuits. The output of the common-mode feedback circuit is connected to the gate of the biasing transistor of the basic amplifier to control the output common-mode voltage. The design was implemented in an AMI 0.5 μm n-well CMOS process that is available through the MOSIS program. The design details of each block follow.

(1) Basic amplifier

The basic amplifier is a common-source differential gain stage with current-source load. Its schematic is shown in Figure 16. The inputs are V_{ip} and V_{in}, and the outputs are V_{olp} and V_{oln}. V_{BP} and V_{BN} are bias voltages provided by the bias generator. Transistor M6b is connected to the CMFB circuit to adjust the output common–mode output voltage. Part of the tail current of the differential pair is provided by a constant current source by transistor M5b so that M6b makes only small adjustments to the circuits. Table 1 shows the transistor sizes of the basic amplifier.

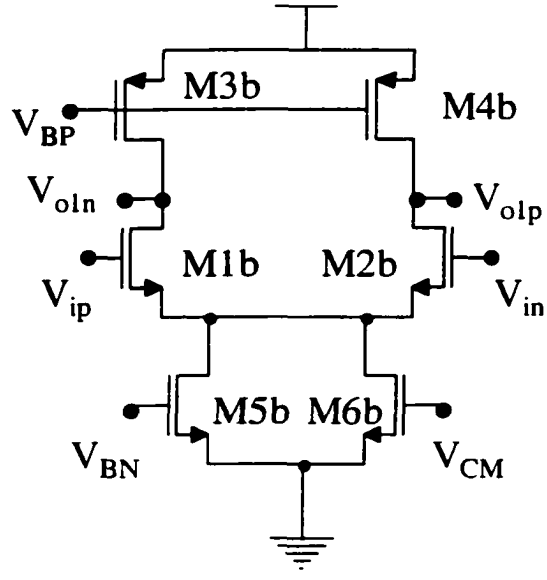


Figure 16. Schematic of the basic amplifier

Table 1 Transistor sizes of the basic amplifier

$(W/L)_{1b}$	$(W/L)_{2b}$	$(W/L)_{3b}$	$(W/L)_{4b}$	$(W/L)_{5b}$	$(W/L)_{6b}$
9u/0.9u	9u/0.9u	11.1u/2.1u	11.1u/2.1u	15.3u/2.1u	15.3u/2.1u

(2) Negative conductance generator

The schematic of the negative conductance generator is shown in Figure 17. It includes the low gain stage A, the negative conductance generating transistors M1c and M7c, and their biasing circuits. The schematic of the low gain stage A is shown in Figure 18. Transistors M2c, M3c, M4c, M8c, M9c, M10c provide constant biasing gate-source voltages for M1c and M7c. By adjusting voltage V_{ctrl}, the biasing current of the negative conductance generator transistors M1c and M7c will be adjusted so that the negative conductance is adjusted. Table 2 shows the transistor sizes of the negative conductance generator. The transistor sizes of the low gain stage A are shown in Table 3.

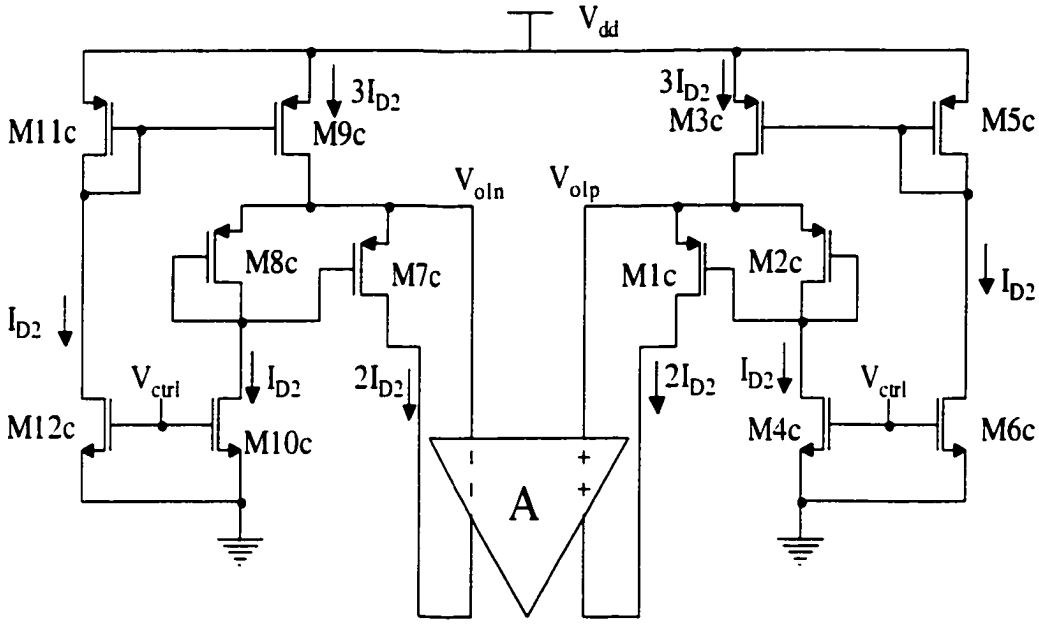


Figure 17. Schematic of the negative conductance generator

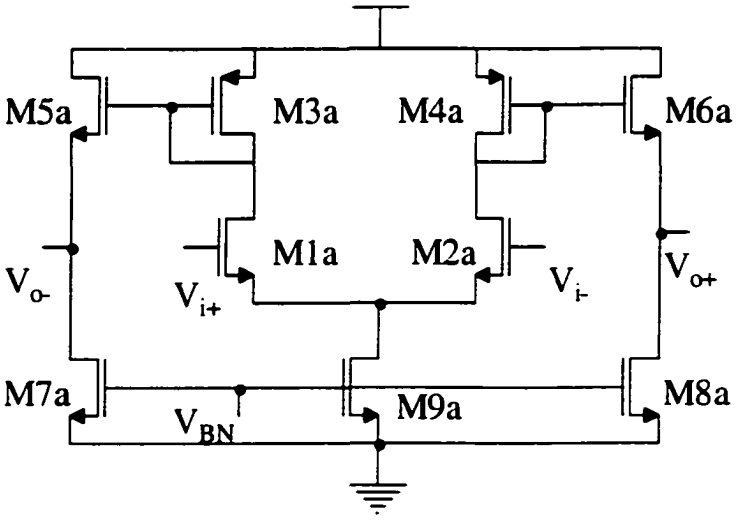


Figure 18. Schematic of the low gain stage A

Table 2 Transistor sizes of the negative conductance generator

$(W/L)_{1c}$, $(W/L)_{7c}$	$(W/L)_{2c}$, $(W/L)_{8c}$	$(W/L)_{3c}$, $(W/L)_{9c}$	$(W/L)_{4c}$, $(W/L)_{10c}$	$(W/L)_{5c}$, $(W/L)_{11c}$	$(W/L)_{6c}$, $(W/L)_{12c}$
324u/0.9u	162u/0.9u	36u/2.1u	84.9u/2.1u	12u/2.1u	30u/2.1u

Table 3 Transistor sizes of the low gain stage A

$(W/L)_{1a}$, $(W/L)_{2a}$	$(W/L)_{3a}$, $(W/L)_{4a}$	$(W/L)_{5a}$, $(W/L)_{6a}$	$(W/L)_{7a}$, $(W/L)_{8a}$	$(W/L)_{9a}$
9.3u/0.6u	3u/0.6u	10.5u/0.6u	15u/2.1u	12.6u/2.1u

(3) Common-mode feedback circuit

As discussed in Section 3.4.3, a common-mode feedback circuit is required to control the output common-mode component in fully differential amplifiers.

Duque-Carrillo [47] indicated that a CMFB network must satisfy the following requirements:

1. To set the output CM component at a preset dc reference level, which is usually where the differential mode gain reaches a maximum value and/or the maximum symmetric voltage (or current) swing is obtained.
2. To process the CM component with a speed and accuracy similar to the ones which the DM component is processed by the differential amplifier.
3. To minimize the interaction of the processing of the CM output component in the DM output component, and Vice versa.

There are two typical approaches to design CMFB circuits a continuous time approach and a switched-capacitor approach. The latter approach is typically only used in switched-capacitor circuits since it introduces clock feedthrough glitches in continuous-time application. In our design, a continuous-time CMFB circuit is used since the differential amplifier works in continuous-time mode.

A CMFB circuit is designed based on the structure reported in [47]. The schematic is shown in Figure 19. Its operation is as follows. Assume a desired common-mode output voltage of V_{cmref} and the input to the CMFB circuit V_{olp} is equal in magnitude, but opposite in sign, to the input V_{oln}. Transistors M8cm, M9cm, and M10cm serve as current sources. Since the two pairs have the same differential voltages being applied, the current in M1cm will be equal to the current in M4cm, while the current in M2cm will equal the current in M3cm. This result is valid independent of the nonlinear relationship between a differential pair's input voltage and its large-signal differential drain currents. As long as the deviation of the voltage V_{olp} from V_{cmref} is equal to the negative of the deviation of the voltage V_{oln} from V_{cmref}, the current through diode-connected M7cm will not change even when large differential signal voltage are present. When a common-mode voltage other than V_{cmref} is present. For example, assume a common-mode signal larger than V_{cmref} is present. This voltage will cause the

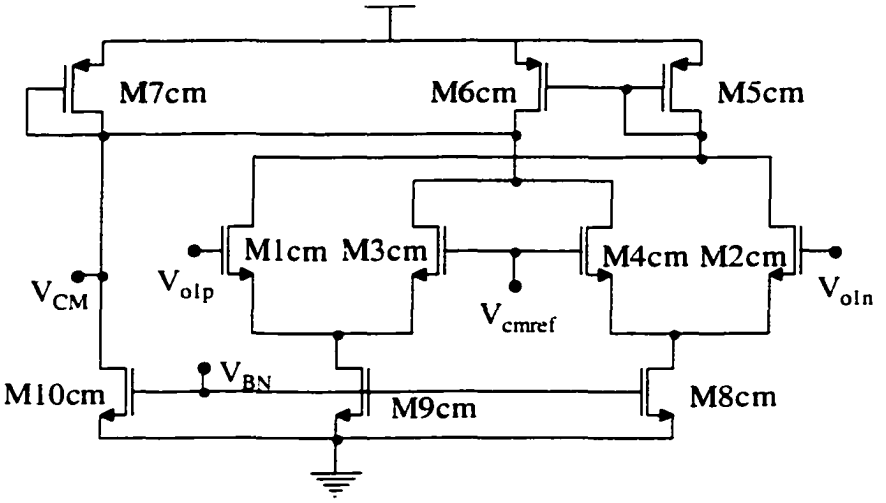


Figure 19. Common-mode feedback circuit

currents in both M3cm and M4cm to change, which causes the current in diode-connected M7cm to change, which in turn causes its voltage V_{CM} to change. V_{CM} is the bias voltage that sets the tail bias current for the basic amplifier. For example, increasing V_{CM} will cause the common-mode voltage to decrease, thus bringing the common-mode voltage back to V_{cmref}. If the output voltage is so large that transistors in the differential pairs turn off then the above description of operation does not remain valid. The size of the differential-pair signals that can be processed without one of the differential-pair signals turning off is maximized if the differential-pair transistors are designed to have large effective gate-source voltages. The transistor sizes of designed CMFB circuit are shown in Table 4.

Table 4 Transistor sizes of the CMFB circuit

$(W/L)_{1cm}$, $(W/L)_{2cm}$, $(W/L)_{3cm}$, $(W/L)_{4cm}$	$(W/L)_{5cm}$, $(W/L)_{6cm}$, $(W/L)_{7cm}$	$(W/L)_{8cm}$, $(W/L)_{9cm}$	$(W/L)_{10cm}$
14.1u/0.6u	21u/1.5u	108u/2.1u	104.4u/2.1u

(4) Bias generator

The bias generator is designed to provide the bias voltages V_{BP} and V_{BN} needed in the basic amplifier, the second amplifier stage and the CMFB circuits. A self-bias structure is used to reduced the process and temperature variation and also provide good supply noise rejection [51][52]. Shown in Figure 20, transistors M5d-M9d form a differential amplifier. The amplifier adjusts V_{BN} so that the voltage VBP is equal to V_{ref}. A bias start up circuit including M14d-M16d and two inverters is added to eliminate the existence of "degenerate" bias point. The start up circuit is needed because if all of the transistors carry zero current when the supply is turned on, they may remain off indefinitely because the loop can support a zero current in all branches. The transistor sizes of the bias generator are shown in Table 5.

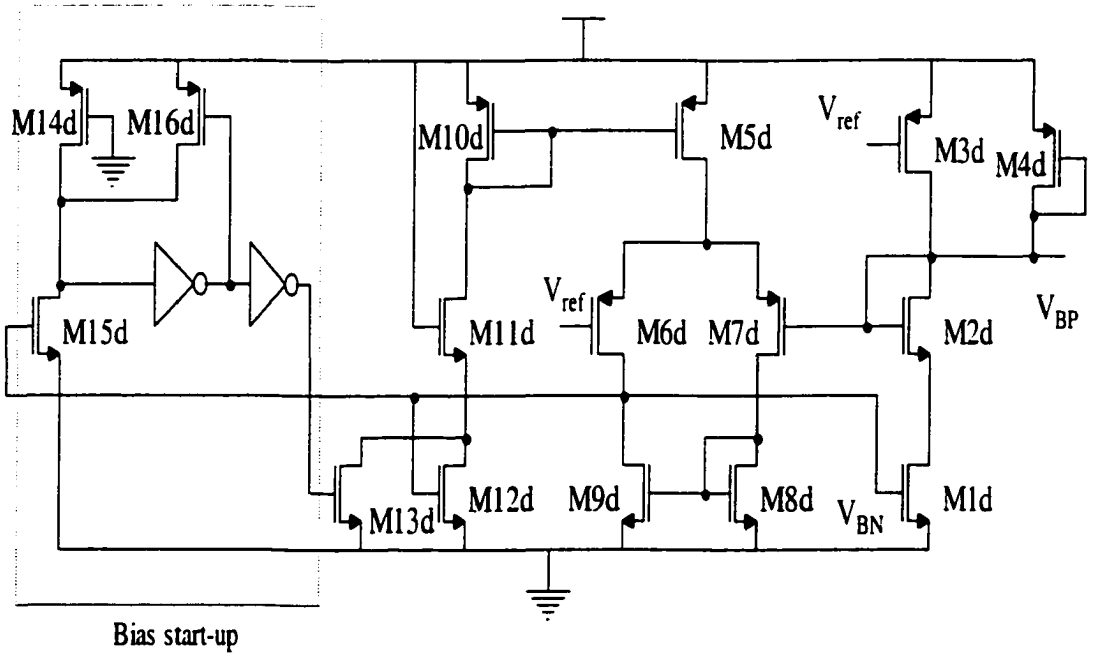


Figure 20. Schematic of the bias generator

Table 5 Transistor sizes of the bias generator

$(W/L)_{1d}$	$(W/L)_{2d}$	$(W/L)_{3d}$	$(W/L)_{4d}$	$(W/L)_{5d}$, $(W/L)_{10d}$	$(W/L)_{6d}$, $(W/L)_{7d}$	$(W/L)_{8d}$, $(W/L)_{9d}$
58.5u/2.1u	34.5u/0.9u	9u/2.1u	16.2u/2.1u	63u/1.2u	54u/1.2u	9u/1.8u
$(W/L)_{10d}$	$(W/L)_{11d}$	$(W/L)_{12d}$	$(W/L)_{13d}$	$(W/L)_{14d}$	$(W/L)_{15d}$	
9.3u/1.8u	15.6u/1.8u	21u/0.6u	1.5u/12.9u	12u/0.6u	1.5u/0.6u	

(5) Second stage

The second stage is a single-ended common source amplifier with diode-connected load. The schematic is shown in Figure 21. The gain of the second stage was designed to be 2.4. The open-loop pole of the second stage was designed to be at a very high frequency by increasing the current. Transistor sizes of the second stage are shown in Table 6.

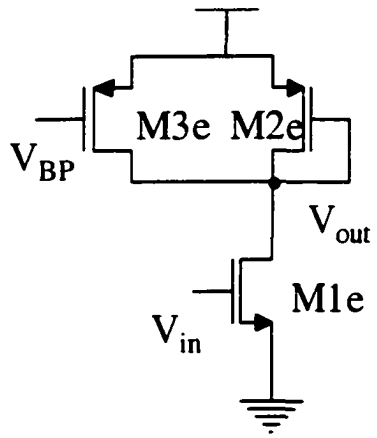


Figure 21. Schematic of the second stage

Table 6 Transistor size of the second stage

$(W/L)_{1e}$	$(W/L)_{2e}$	$(W/L)_{3e}$
72.9u/0.6u	36.9u/0.6u	259.2u/0.6u

3.4.7 DC gain enhancement

Although the amplifier is a two-stage amplifier, DC gain enhancement is achieved in the first stage by adding a negative conductance at the output nodes of the basic amplifier. The negative conductance added at the output nodes of the basic amplifier does not affect the DC gain of the second stage. Define the first stage as the basic amplifier plus the Negative Conductance Generator. The overall DC gain of the amplifier is

$$A_{vd,tot} = A_{vd1} \bullet A_{vd2} \tag{52}$$

where A_{vd1} is the DC gain of the first stage, and A_{vd2} is the DC gain of the second stage shown in Figure 21. A_{vd2} is derived as

$$A_{vd2} = \frac{-g_{m1e}}{g_{m2e} + g_{ds1e} + g_{ds2e} + g_{ds3e}} \approx \frac{-g_{m1e}}{g_{m2e}} \tag{53}$$

A_{vd1} is derived based on the half circuit of the first stage shown in Figure 22. Assume the biasing current for the basic amplifier is I_{D1} and the biasing current for the Negative Conductance Generator is I_{D2}. The small signal equivalent circuit of the half circuit is shown in Figure 23. The differential

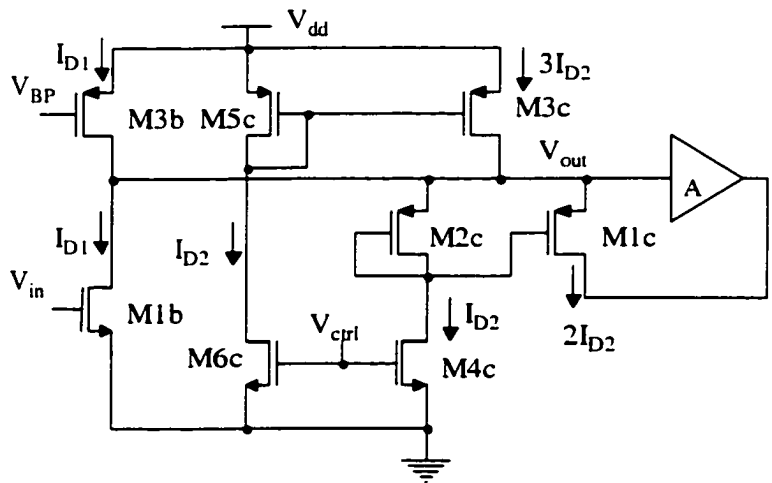


Figure 22. The half circuit of the first stage

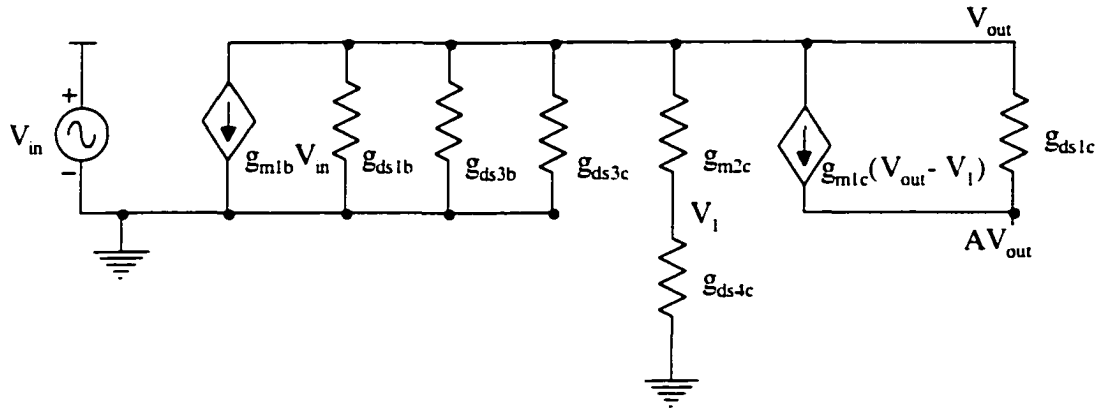


Figure 23. The small signal equivalent circuit of the half circuit of the first stage

gain of the first stage can be derived as

$$A_{vd1} = \frac{V_{out}}{V_{in}} = \frac{-g_{m1b}}{g_{ds1b} + g_{ds3b} + g_{ds3c} + k(g_{m1c} + g_{m2c}) + (1 - A)g_{ds1c}} \tag{54}$$

where

$$k = \frac{g_{ds4c}}{g_{ds4c} + g_{m2c}} \tag{55}$$

A is the DC gain of the low gain stage A. The schematic of the low gain stage A is shown in Figure 18. The DC gain of the low gain stage A is derived as

$$A = \frac{g_{m1a}}{g_{m3a}} \bullet \frac{g_{m5a}}{g_{ma5a} + g_{mb5a}} \tag{56}$$

Transistor M2c has the same gate-source voltage as that of transistor M1c but its size is half thus g_{m2c} is ½ of g_{m1c}. Expression (54) can be simplified as

$$A_{vd1} = \frac{V_{out}}{V_{in}} = \frac{-g_{m1b}}{g_{ds1b} + g_{ds3b} + g_{ds3c} + k_1 g_{m1c} + (1 - A)g_{ds1c}} \tag{57}$$

where

$$k_1 = \frac{3}{2}k = \frac{3}{2}\frac{g_{ds4c}}{(g_{ds4c} + g_{m2c})} \tag{58}$$

From the expression (55), if $g_{ds4c} << g_{m2c}$, k will be a small number and the positive g_{m1c} term in the denominator of the gain expression (54) can be ignored. The DC gain of the first stage becomes

$$A_{vd1} = \frac{-g_{m1b}}{g_{ds1b} + g_{ds3b} + g_{ds3c} + (1-A)g_{ds1c}} \tag{59}$$

3.4.8 Relationship between DC gain and the control voltage V_{ctrl}

In our design, the negative conductance is adjustable by changing the control voltage V_{ctrl} thus changing the bias current I_{D2} of the negative conductance transistors Mc1 and Mc7. The relationship between I_{D2} and the control voltage V_{ctrl} is defined as

$$I_{D2} \approx \frac{\mu_n C_{ox}(W/L)_{4c}}{2}(V_{ctrl} - V_{tn})^2 \tag{60}$$

Both g_{ds1c} and $k_1.g_{m1c}$ change when the control voltage V_{ctrl} changes. In what follows, it will be assumed that

$$g_{ds} = \lambda I_D \tag{61}$$

$$\lambda_n = \lambda_p = \lambda \tag{62}$$

The relationship between the DC gain and the control voltage V_{ctrl} depends on how g_{ds4c} compares with g_{m2c}.

Case 1. $g_{ds4c} << g_{m2c}$

The DC gain of the first stage is described by the expression (59). The gain will go to infinity if the denominator of the expression (59) becomes zero. The roots of the denominator of the expression (59) can be found by solving following equation

$$2I_{D1}\lambda + 3\lambda I_{D2} + 2(1-A)\lambda I_{D2} = 0 \tag{63}$$

Substitute equation (60) to equation (63), a manipulation of above equations gives the following simpler but equivalent relationship

$$(V_{ctrl} - V_{tn})^2 = \frac{4I_{D1}}{(2A-5)\mu_n C_{ox}(W/L)_{4c}} \tag{64}$$

Since The control voltage V_{ctrl} must be greater than the threshold voltage V_{tn} to turn on transistor M4c. The control voltage V_{ctrl} can be solved from equation (64).

$$V_{ctrl} = 2\sqrt{\frac{I_{D1}}{(2A-5)\mu_n C_{ox}(W/L)_{4c}}} + V_{tn} \tag{65}$$

Expression (65) shows that only one value of V_{ctrl} will make the denominator of the gain expression (59) be zero and A_{vd1} be infinite if $g_{ds4c} << g_{m2c}$.

Case 2. g_{ds4c} is compatable with g_{m2c}

If g_{ds4c} is compatable with g_{m2c} , the DC gain of the first stage is described with the expression (57). The g_{m1c} term in the denominator of expression (57) should be taken into account.

Since

$$g_m = \sqrt{2\mu C_{ox}(W/L)I_D} \tag{66}$$

The roots of the denominator of the expression (57) can be found by solving following equation

$$2I_{D1}\lambda + (5-2A)\lambda c_1(V_{ctrl} - V_{tn})^2 + 3\frac{\lambda\sqrt{c_2}I_{D2}}{\lambda\sqrt{I_{D2}} + \sqrt{c_3}} = 0 \tag{67}$$

where

$$c_1 = \frac{\mu_n C_{ox}}{2}(W/L)_{4c} \tag{68}$$

$$c_2 = \mu_p C_{ox}(W/L)_{1c} \tag{69}$$

$$c_3 = 2\mu_p C_{ox}(W/L)_{2c} \tag{70}$$

The following simpler but equivalent relationship is obtained by substituting equation (60) to equation (67).

$$2I_{D1}\lambda + (5-2A)\lambda c_1(V_{ctrl}-V_{in})^2 + 3\frac{\lambda c_1\sqrt{c_2}(V_{trl}-V_{in})^2}{\lambda\sqrt{c_1}(V_{ctrl}-V_{in})+\sqrt{c_3}} = 0 \tag{71}$$

Assume $y = V_{ctrl} - V_{in}$

A manipulation of equation (71) gives the following equivalent relationship

$$\lambda c_1^{1.5}(5-2A)y^3 + c_1[3\sqrt{c_2} + (5-2A)\sqrt{c_3}]y^2 + 2I_{D1}\lambda\sqrt{c_1}y + 2I_{D1}\sqrt{c_3} = 0 \tag{72}$$

Expression (72) shows that there are multiple values of V_{ctrl} that will make the denominator of the gain expression (54) be zero and A_{vd1} be infinite if g_{ds4c} is compatable with g_{m2c}.

HSPICE simulation results of the designed amplifier verified the above statements. Figure 24 shows the relationship between the control voltage V_{ctrl} and the output conductance of the first amplifier stage when the positive transconductance g_{m1c} term is ignored or included. Curve 1 shows the positive conductance g_{dsp} which is equal to (g_{ds1b}+g_{ds3b}+g_{ds3c}). Curve 2 shows the summation of the positive conductance g_{dsp} plus the positive transconductance $k_1 g_{m1c}$ term. Curve 3 shows negative conductance g_{dsn} =(1-A).g_{ds1c}. Curve 4 shows the total output conductance of the first stage g_{ds_tot} which is

$$g_{ds\_tot} = g_{dsp} + k_1 \cdot g_{m1c} - (A-1)g_{ds1c} \tag{73}$$

Figure 24 shows that without the effect of g_{m1c}, Curve 1 and Curve 3 have only one interception point. This means only one value of V_{ctrl} makes the negative conductance equal to the positive conductance and the overall DC gain of the first amplifier stage goes to infinity. With g_{m1c} term, Curve 2 and Curve 3 have two interception points. This means that two values of V_{ctrl} make the

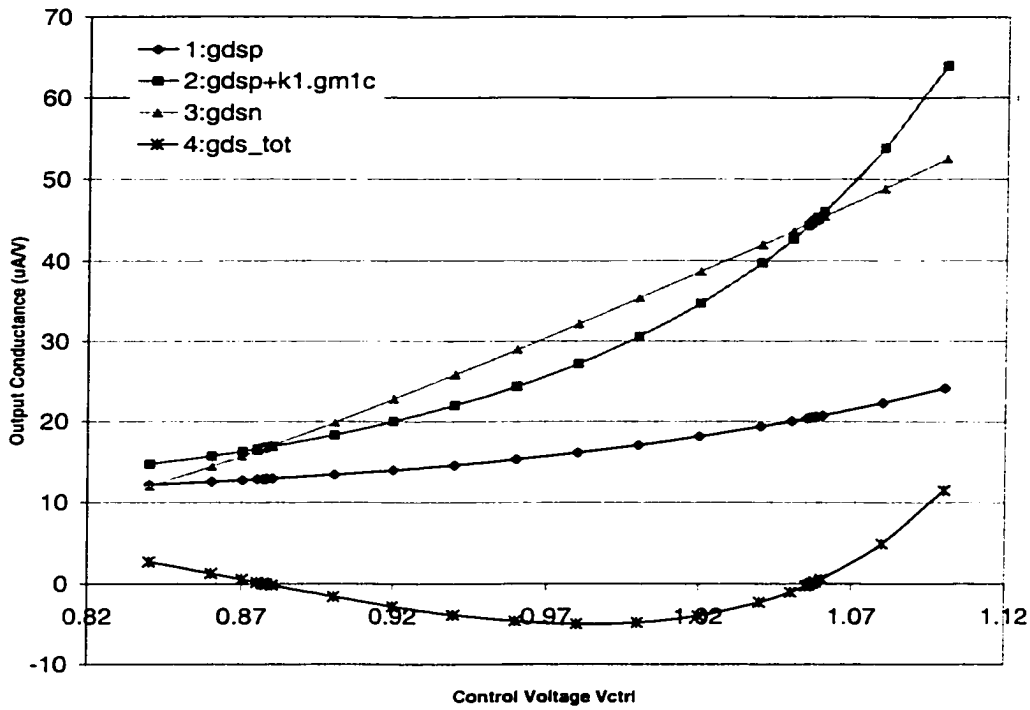


Figure 24. The relationship between the control voltage V_{ctrl} and the output conductance of the amplifier

negative conductance equals the positive conductance plus $k_1.g_{m1c}$ term thus the total output conductance becomes zero and overall DC gain of the first amplifier stage becomes infinite. With the g_{m1c} term, Curve 4 shows that the total output conductance of the first stage becomes zero twice for a control voltage range from 0.84V to 1.1V.

The DC gain of the amplfier is sensitive to process variations due to the effect of $k_1.g_{m1c}$. Because both g_{ds1c} and $k_1.g_{m1c}$ vary with the control voltage V_{ctrl}. If the $k_1.g_{m1c}$ term becomes bigger than $(1\text{-}A)g_{ds1c}$, not enough negative conductance will be generated to compensate the positive conductance plus $k.g_{m1c}$ term no matter how to adjust the control voltage. In this situation, the amplifier can only achieve limited gain enhancement because there is no control voltage V_{ctrl} can make the DC gain go to infinity.

The designed amplifier was simulated with a 3 Volts supply voltage. Figure 25 shows the simulated DC gain versus the control voltage V_{ctrl} for different process corners. For each process corner there are two DC gain peaks. This indicates there are two values of V_{ctrl} which makes the DC gain go to infinity. Between the two peaks the total effective output conductance of the amplifier is a negative value and the amplifier has a RHP open loop pole. However, at the slow process corner, two infinite DC gain points are very close to each other implying the V_{ctrl} range for RHP open-loop pole is very narrow.

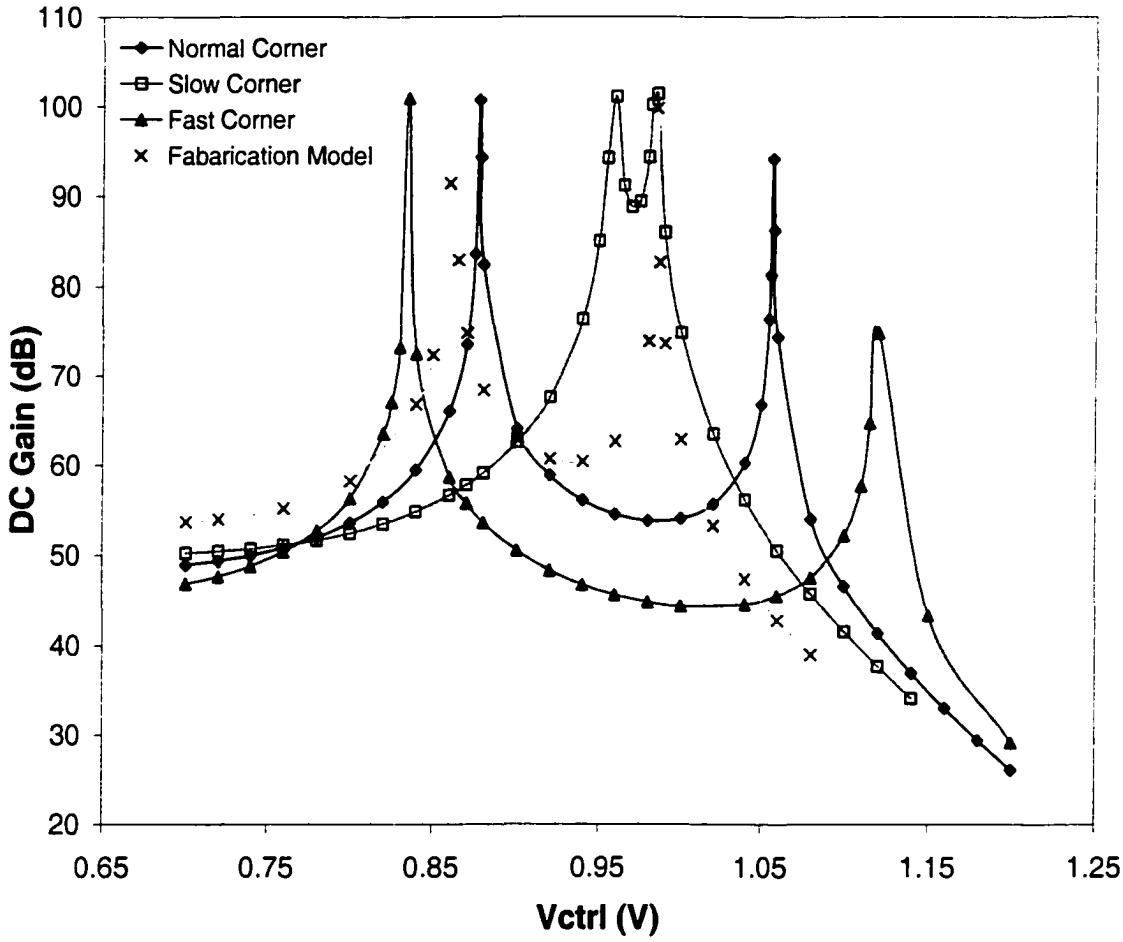


Figure 25. Simulated DC gain over process corners at T=25 ° C

In addition, the DC gain of the amplifier is also sensitive to the temperature variation because of the effect of $k_1.g_{m1c}$. The temperature dependence of MOS transistor threshold voltage [53] is given by

$$\frac{dV_{T0}}{dT} = \frac{d\phi_{GB}}{dT} + (2 \pm \frac{\gamma}{\sqrt{2|\phi_F|}}) \frac{d\phi_F}{dT} \tag{74}$$

with + for an NMOS and – for a PMOS. The temperature dependence of ϕ_F is given by

$$\frac{d\phi_F}{dT} = \frac{1}{T}[\phi_F \pm (\frac{3}{2}\frac{kT}{q} + \frac{E_{g0}}{2q}] \tag{75}$$

in which – is used for an NMOS and + for a PMOS.

The temperature coefficient of the mobility is given by

$$\frac{1}{\mu}(\frac{d\mu}{dT}) = - \frac{n_\mu}{T} \tag{76}$$

For low doping level, the value of n_μ is about 1.5. For a MOS transistor in saturation, the expression of the current in its simplest form is given by

$$i_{dsat} = \frac{\mu cox W}{2L}(V_{gs} - V_T)^2 \tag{77}$$

The temperature coefficient of the current is derived by taking the derivative with respect to temperature [53], which yields

$$\frac{1}{i_{dsat}}(\frac{di_{dsat}}{dT}) = - \frac{n_\mu}{\mu} - + \frac{-2}{V_{gs} - V_T}(\frac{dV_T}{dT}) \tag{78}$$

Since the V_T of a PMOS transistor has a positive temperature coefficient, the second term is negative. The current of a PMOS has a negative temperature coefficient. For a PMOS transistor, the current increases when temperature decreases.

Based on g_{ds} expression (61), the temperature coefficient of g_{ds} is derived as

$$\frac{1}{g_{ds}}\frac{dg_{ds}}{dT} = \frac{1}{id_{sat}}\frac{di_{dsat}}{dT} \tag{79}$$

Based on g_m expression (66), the temperature coefficient of g_m is derived as

$$\frac{1}{g_m}\frac{dg_m}{dT} = \frac{1}{2}\left(\frac{1}{\mu}\frac{d\mu}{dT} + \frac{1}{id_{sat}}\frac{di_{dsat}}{dT}\right) \tag{80}$$

Since the negative conductance transistor Mc1 is a PMOS transistor, both g_{m1c} and g_{ds1c} have a negative temperature coefficient but change with the temperature differently.

Figure 26 shows simulation results of temperature effects on DC gain at the slow process corner. At T = 30° C and T = 40° C, the $k_1.g_{m1c}$ term is dominant. the negative conductance is not big enough to compensate the positive conductance plus $k_1.g_{m1c}$ term when the control voltage is adjusted.

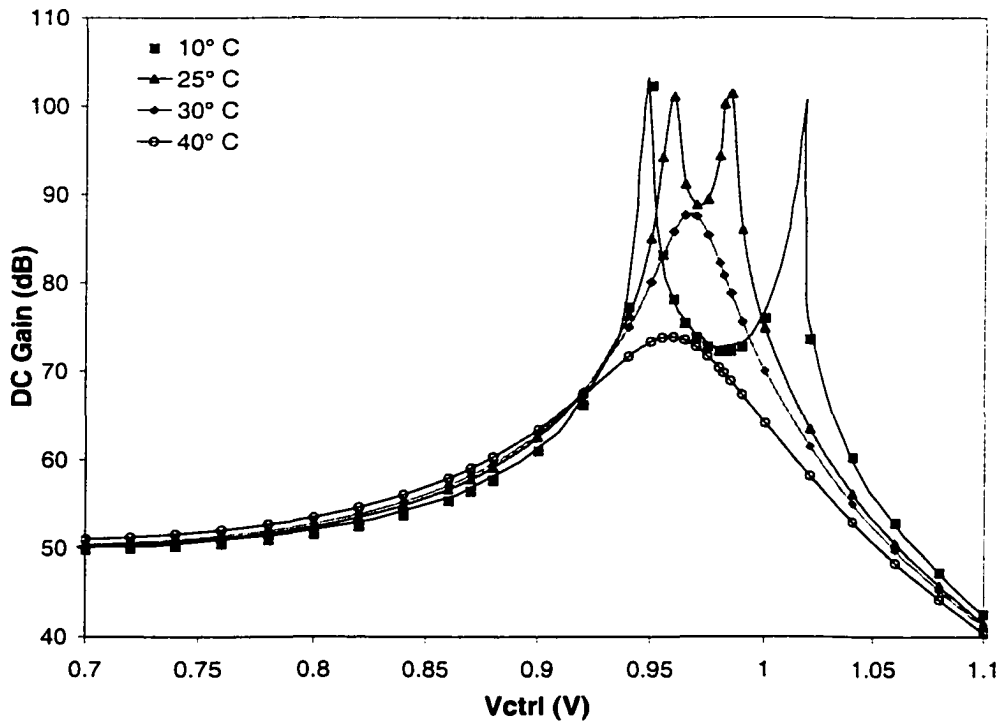


Figure 26. Simulated temperature effects on DC gain

The DC gain is enhanced somehow but cannot reach infinite. At lower temperatures T = 25° C and T = 10° C, the effects of $k_1.g_{m1c}$ term become less dominant. There are two control voltage values make the DC gain goes to infinity. At T = 10° C, the amplifier showed wider control voltage range in which the total effective output conductance of the amplifier is a negative value and the amplifier has a RHP open loop pole.

3.4.9 High frequency behavior

In the prototype amplifier design, compensation of the amplifier is done by shifting more of the power from the first stage to the second stage and adding a 1.5pF compensation capacitor Cc at the output of the first stage to ground. Referring to the schematics of the first stage and the second stage of the amplifier, the simplified small-signal model shown in Figure 27 can be used to analysis the high frequency behavior of the amplifier. In the small signal model, we have

$$R_1 = \frac{1}{g_{ds1b} + g_{ds3b} + (1-A)g_{ds1c}} \tag{81}$$

$$C_1 = Cc + C_{db1b} + C_{db3b} + C_{gs1e} \tag{82}$$

$$R_2 = \frac{1}{g_{ds1e} + g_{m2e} + g_{ds3e}} \approx \frac{1}{g_{m2e}} \tag{83}$$

$$C_2 = C_{db1e} + C_{db2e} + C_{db3e} + C_{L2} \tag{84}$$

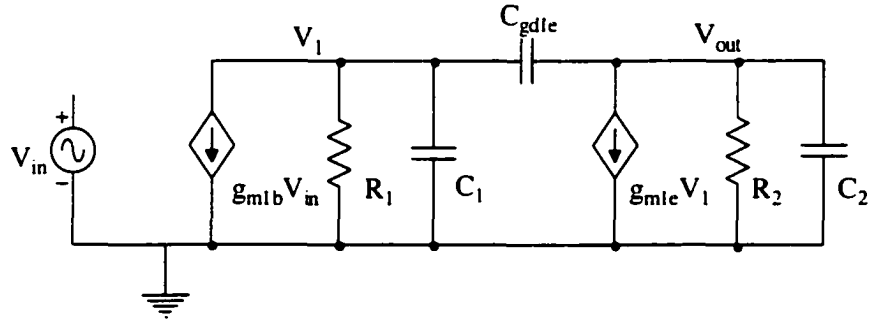


Figure 27. A small-signal model of the amplifier used for frequency analysis

In expression (84), C_{L2} is the load capacitance at the output node of the second stage. To achieve DC gain enhancement R_1 is designed much larger than R_2.

Perform nodal analysis at the nodes designed by V_1 and V_{out}, the following transfer function is obtained:

$$\frac{v_{out}}{v_{in}} = \frac{g_{m1b}g_{m1e}R_1R_2(1-\frac{sC_{gd1e}}{g_{m1e}})}{S^2R_1R_2[(C_1+C_2)C_{gd1e}+C_1C_2)+s(R_1R_2C_{gd1e}g_{m1e}+R_2(C_{gd1e}+C_2)+R_1(C_{gd1e}+C_1)]} \tag{85}$$

Assume the two poles are real and widely separated. The denominator D(s) can be expressed as

$$D(s) = (1+\frac{s}{\omega_{p1}})(1+\frac{s}{\omega_{p2}}) \cong 1+\frac{s}{\omega_{p1}}+\frac{s^2}{\omega_{p2}} \tag{86}$$

Setting the coefficients of (85) equal to the coefficients of (86) and solving for ω_{p1} and ω_{p2} results in the following relationships. The dominant pole, ω_{p1}, is given by

$$\omega_{p1} \cong \frac{1}{R_1[C_1+C_{gd1e}(1+g_{m1e}R_2)]+R_2(C_2+C_{gd1e})} \cong \frac{1}{R_1C_{L1}} \tag{87}$$

where

$$C_{L1} \cong C_1+C_{gd1e}(1+g_{m1e}R_2) \tag{88}$$

whereas the nondominator pole, ω_{p2}, is given by

$$\omega_{p2} \cong \frac{g_{m1e}C_{gd1e}}{C_1C_2+C_2C_{gd1e}+C_1C_{gd1e}} \cong \frac{g_{m1e}}{C_1+C_2} \tag{89}$$

The zero ω_z is located in the right half plane and is given by

$$\omega_Z = \frac{g_{m1e}}{C_{gd1e}} \tag{90}$$

Because g_{m1e} is designed very large and C_{gd1e} is small, the zero ω_z will be located at very high frequency and is not a problem.

Increasing R_1 moves the dominant pole ω_{p1} to a lower frequency without affecting the second pole ω_{p2}. This effect makes the op amp more stable. The Gain-bandwidth-product of the amplifier is given by

$$GB \equiv A_{vdtot}\omega_{p1} \equiv A_{vd1} \cdot A_{vd2} \cdot \omega_{p1} = g_{m1b}R_1 \frac{1}{R_1 C_{L1}} g_{m1e}R_2 = \frac{g_{m1b}}{C_{L1}} g_{m1e}R_2 \qquad (91)$$

In the prototype amplifier design, the amplifier is implemented as unity-gain feedback configuration with on-chip feedback resistors. Two output buffers are connected to the closed-loop amplifier outputs in order to drive 10pF capacitance load. Therefore, the amplifier's actual load is the output buffer. Two source followers are designed as output buffers and are driven by the feedback amplifier. The frequency response of the source follower is analyzed as follow. Consider the source follower depicted in Figure 28a, where R_s is the input impedance, C_s is the input capacitance, and C_{Lf} represents the total capacitance seen at the output node to ground, including C_{bs1f}. Neglecting body effect for simplicity and using the equivalent circuit shown in Figure 28b, we have

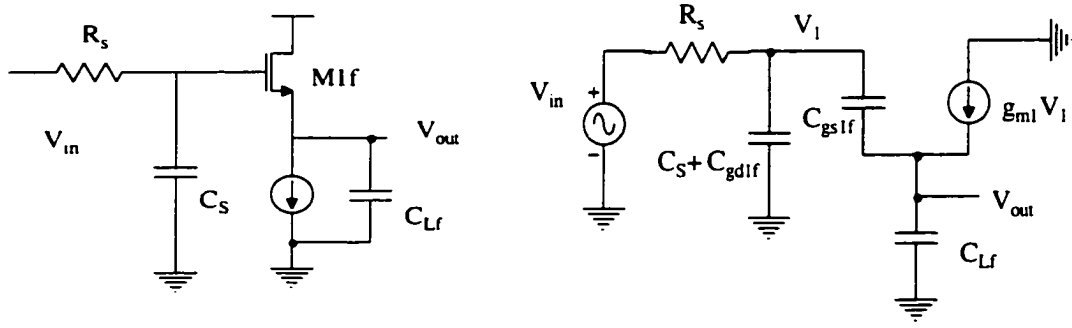


Figure 28. (a) Source follower, (b) high frequency equivalent circuit.

$$\frac{V_{out}}{V_{in}} = \frac{g_{m1f} + C_{gs1f}s}{R_s[C_{gs1f}C_{Lf} + C_{gs1f}C_{gd1f} + (C_{gd1f} + C_s)C_{Lf}]s^2 + [g_{m1f}R_s(C_{gd1f} + C_s) + C_{Lf} + C_{gs1f}]s + g_{m1f}} \tag{92}$$

If the two poles of source follower are assumed far apart, then the dominant pole is

$$\omega_{p1} \approx \frac{g_{m1f}}{g_{m1f}R_s(C_{gd1f} + C_s) + C_{Lf} + C_{gs1f}} = \frac{1}{R_s(C_{gd1f} + C_s) + \dfrac{C_L + C_{gs1f}}{g_{m1f}}} \tag{93}$$

Based on expression (93), increasing R_s, C_s and C_{Lf} will reduce the bandwidth of the source follower. In the prototype amplifier design, R_s is equal to the output impedance of the second stage R2 which is about 400Ω. C_s is equal to the output capacitance of the second stage which is about 1pF.

Unfortunately, in this prototype design, the second pole of the amplifier was designed at not very high frequency. The unity-gain frequency of the amplifier is lower than GB. The amplifier does not roll off with –6dB/Octave and the bandwidth of the feedback amplifier is not equal to β.GB. In addition, the bandwidth of the output buffer was less than the bandwidth of the feedback amplifier when the buffer is driven the 10pF load thus masking the amplifier's actual frequency response. Figure 29 shows simulated open-loop frequency response of the amplifier and the frequency response after the output buffer when it drives a 10pF capacitance load. The bandwidth of the buffer is less than the unity gain frequency of the amplifier. Figure 30 shows simulated closed-loop frequency response of the amplifier and the frequency response after the output buffer when it drives a 10pF capacitance load. The bandwidth of the buffer is less than the cutoff frequency of the feedback amplifier.

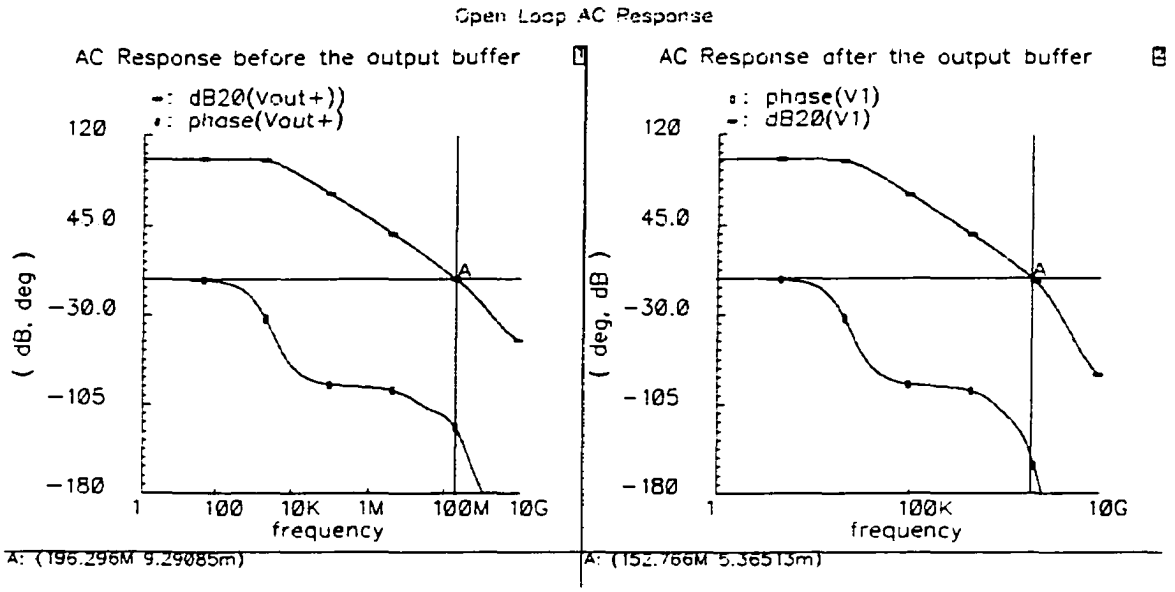


Figure 29. Simulated Open loop frequency response, Vout+: output of the amplifier, V1: output of the buffer.

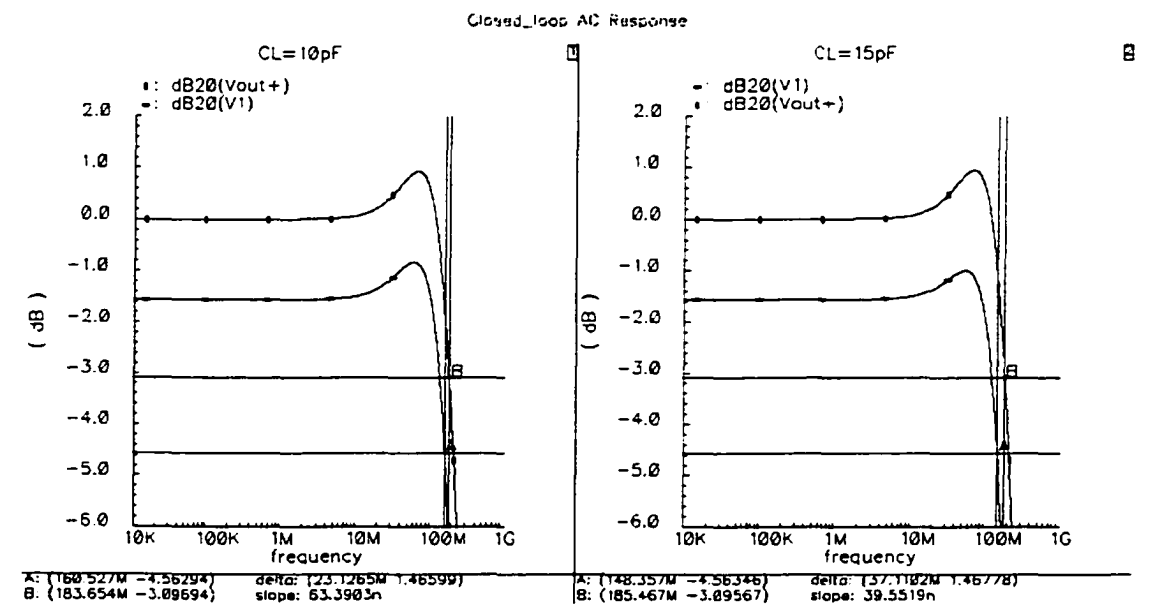


Figure 30. Simulated closed-loop frequency response with different capacitance loads, Vout+: output of the amplifier, V1: output of the buffer

3.5 Conclusion

A new negative conductance gain enhancement scheme is proposed. The proposed circuit generates a negative conductance that is only function of g_{ds} of the compensating device and not related to g_m. Therefore, a negative g_{ds} can realistically match positive g_{ds} terms and the tracking requirements for achieving very high DC gain are less stringent than for the existing –gm gain enhancement schemes. A prototype high gain fully differential CMOS operational amplifier was designed, laid out, and fabricated based on the proposed negative conductance voltage gain enhancement technique. Design details were discussed. DC gain enhancement and the high frequency behavior of the amplifier were analyzed.

CHAPTER 4. EXPERIMENTAL RESULTS OF HIGH GAIN AMPLIFIER

A prototype two-stage fully differential high gain amplifier was designed based on the proposed negative conductance gain enhancement technique to validate the fundamental performance characteristics of the negative conductance gain enhancement technique. The amplifier was fabricated using the AMI Semiconductor (AMIS) 0.5um AMI_C5N process available through MOSIS. The die was packaged in a 40-pin DIP ceramic package. For this process the maximum rated voltage supply is 5 Volts, however, the amplifier was designed for reliable operation at 3 Volts. Following the design and fabrication of the prototype, the amplifier was tested and characterized for DC gain, output swing, power etc.

4.1 Layout

The prototype amplifier die photo is shown in Figure 31. The amplifier was laid out with the second amplifier stages symmetrically around the basic amplifier and the Negative Conductance Generators (NCG) symmetrically around the low gain stage A. The amplifier was implemented to have a closed-loop gain of one with four on-chip feedback resistors. Two output buffers were implemented to drive a 10pF capacitance load and were connected at the output of the feedback amplifier. The feedback resistors were implemented using a poly2 layer inside high resistance implant layer. Each resistor was designed to be 5kΩ. Two 1.5pF compensation capacitors which are connected at the output of the first stage to ground were implemented using poly1-poly2 capacitance. The die was packaged in a DIP 40-pin ceramic package. The total active area of the amplifier and two output buffers and four feedback resistors is $0.077mm^2$.

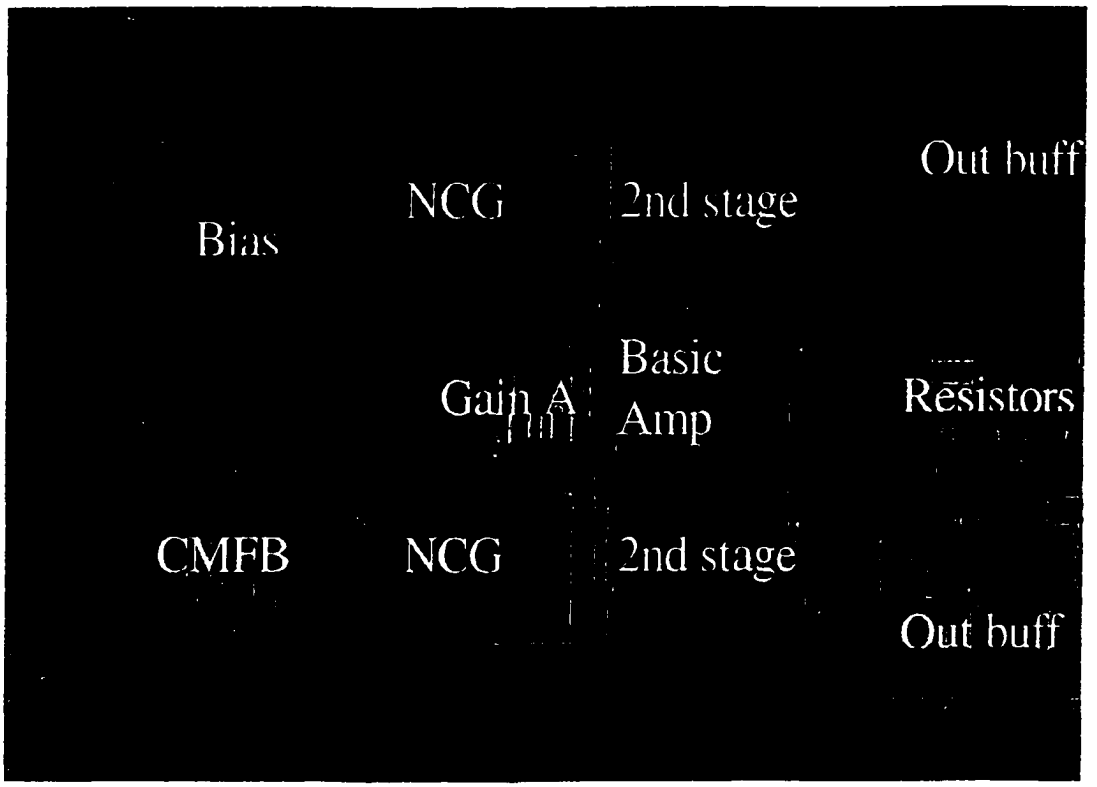


Figure 31. Die photo of prototype amplifier

4.2 DC Gain

4.2.1 DC gain measurement at the room temperature

The open-loop DC gain was measured with the feedback circuit of Figure 32 by applying a low frequency differential square wave signal V_{in} and V_{ip} generated using a Hewlett Packard HP3245A universal source. The differential input signals V_{i+} and V_{i-} at the op amp's inputs are amplified by an off-chip amplifier A2 with a gain of 185. The output signals V_{op} and V_{on} were also measured. The open-loop differential DC gain is given by the expression

$$A_0 = \frac{V_{op} - V_{on}}{V_{i+} - V_{i-}} = \frac{V_{op} - V_{on}}{V_{oA2} / A_2} \tag{94}$$

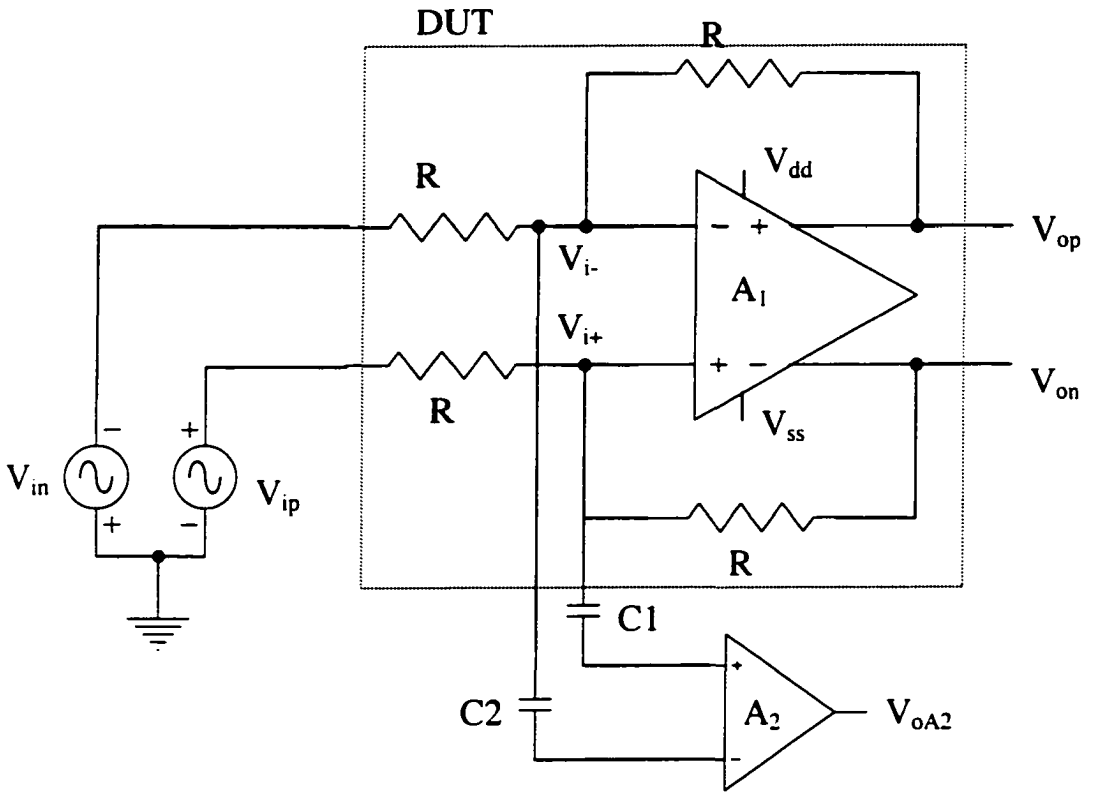


Figure 32. Test setup for open-loop DC gain measurement

The amplifier was tested with ±1.5 V supply voltages generated from the HP E3631A. The control voltage V_{ctrl} for adjusting the DC gain was also generated from the HPE3631A by connecting a 100 KOhm potentiometer to –1.5 Volts. C1 and C2 are used to reduce offset effect of amplifier A2. V_{ctrl} was varied and the DC gain was measured different values of V_{ctrl}.

A 100Hz 100mV square wave differential input signal was applied at V_{ip} and V_{in} to measure the DC gain. Figure 33 shows the differential output signal V_{op}-V_{on} (Math) and the amplified differential input signal V_{oA2} (Ch3) for a control voltage V_{ctrl} of –0.75871 Volt. The differential input signal is in phase with the differential output signal. The open-loop DC gain is 80.24dB.

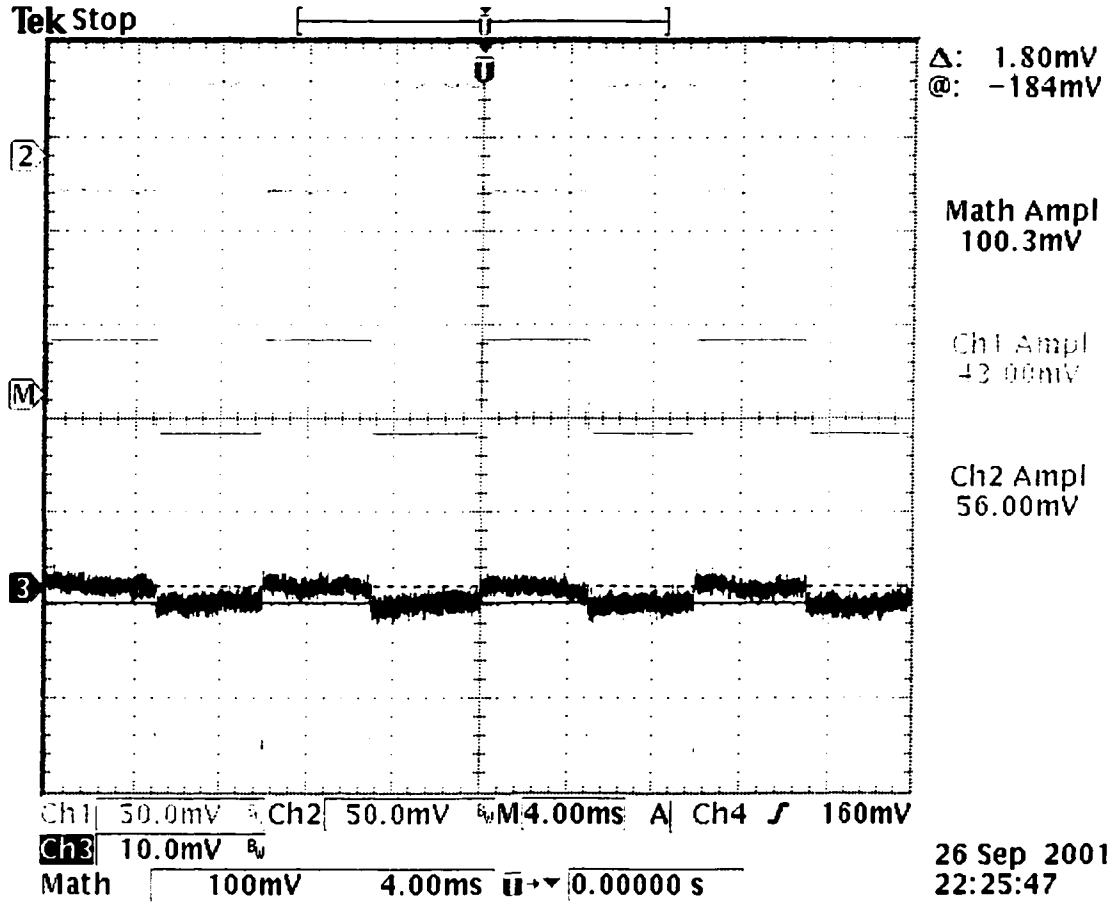


Figure 33. Open-loop DC gain measurement results. The differential output signal (math) and the amplified differential input signal (ch3) with V_{ctrl}=-0.75871 V

Figure 34 shows the differential output signal V_{op}-V_{on} (Math) and the amplified differential input signal V_{oA2} (Ch3) for a control voltage V_{ctrl} of –0.74507 Volt. The differential input signal is out of phase with the differential output signal and the open-loop DC gain is 83.76dB. This indicates the total effective output conductance of the amplifier is negative and the amplifier has a RHP open loop pole.

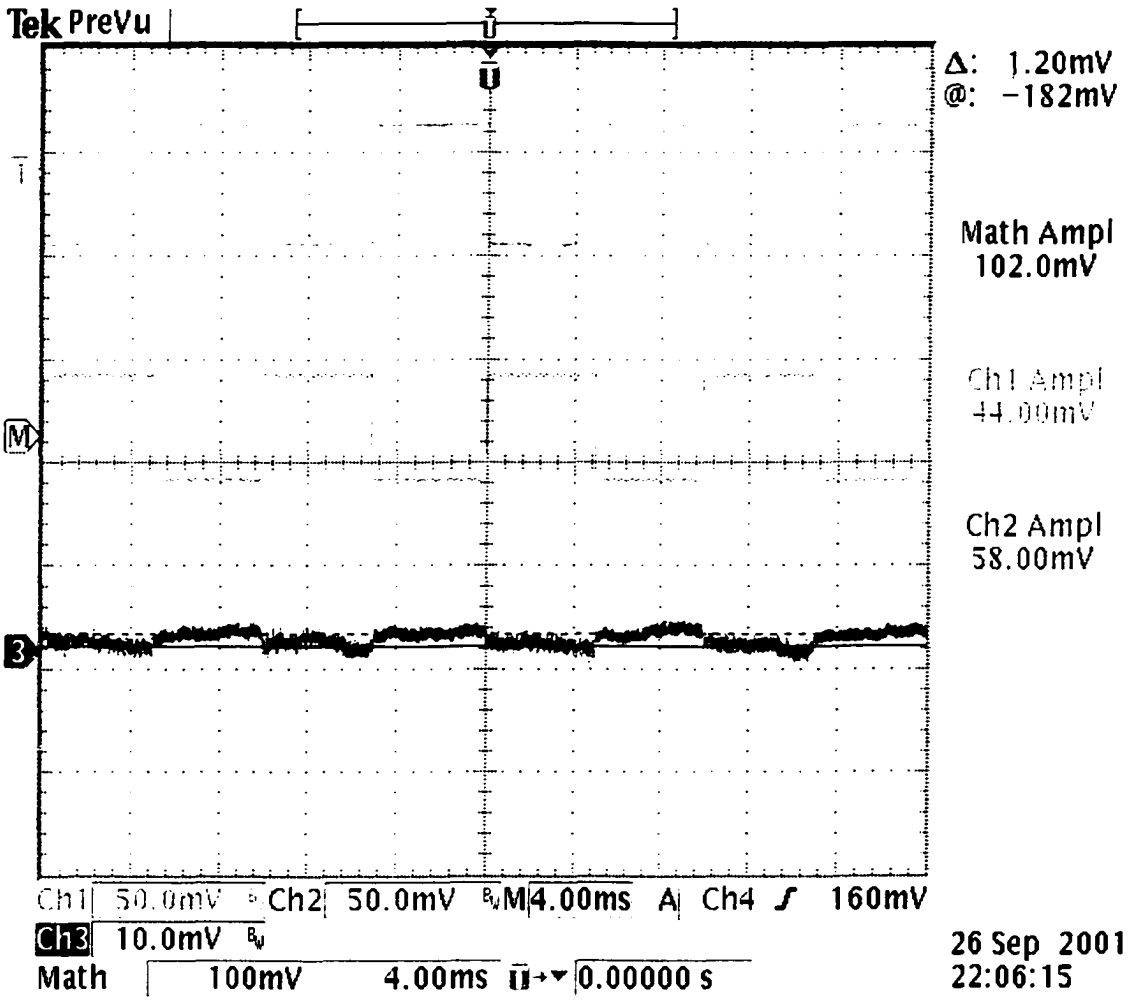


Figure 34. Open-loop DC gain measurement results. The differential output signal (math) and the amplified differential input signal (ch3) with V_{ctrl} = –0.74507 V.

The DC gain is adjustable with the control voltage. Figure 35 shows measured differential open-loop DC gain versus the control voltage V_{ctrl} at room temperature. The DC gain goes to infinity at two values of V_{ctrl}. The overall effective output impedance of the first stage is a negative value for a control voltage range of 13mV.

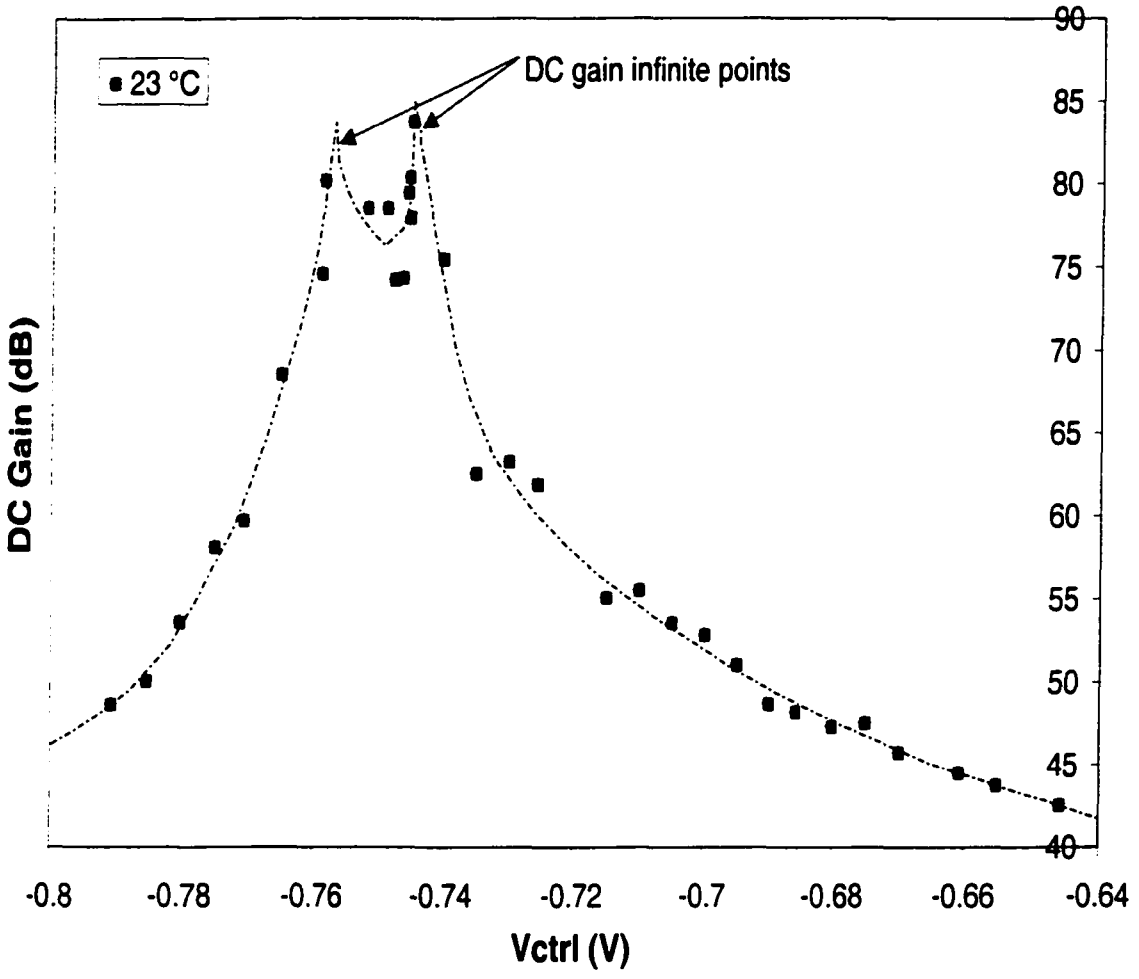


Figure 35. Measured DC gain versus the control voltage V_{ctrl} at room temperature

4.2.2 Process variation effects on the DC gain

Some of the fabricated amplifiers did not show great gain enhancement when adjusting control voltage V_{ctrl}. One such testing result is shown in Figure 36. The overall effective output conductance of the first stage is always positive for all values of the control voltage and correspondingly differential input signals were always in phase with the differential output signals. The DC gain is slightly enhanced because of the effect of $k_1.g_{m1c}$ and not enough negative conductance was generated.

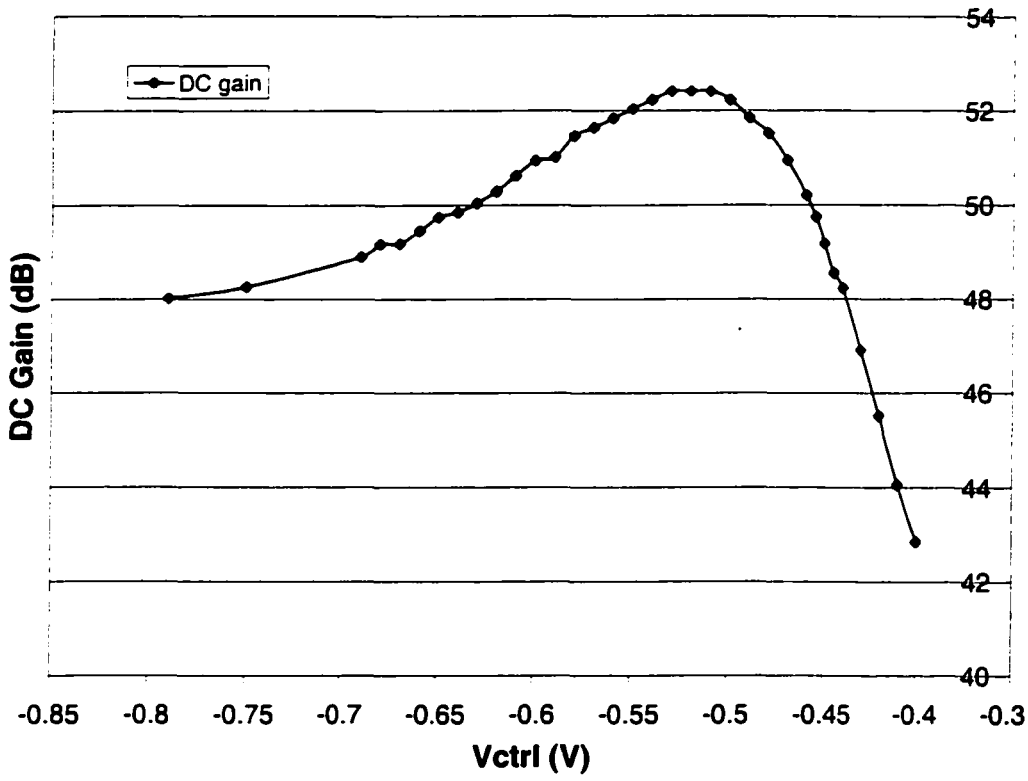


Figure 36. Measured DC gain versus control voltage Vctrl (no phase reversal)

4.2.3 Temperature effects on the DC gain

The DC gain of the amplifier is sensitive to temperature variations because of the bias scheme used in this prototype design. One amplifier was tested at 23 °C and 0 °C respectively in order to show temperature effects on the DC gain. The results are shown in Figure 37. At 23 °C, there are two control voltage values corresponding to infinite DC gain points. The control voltage range for a negative total effective output conductance of the first stage is about 45mV. When the amplifier was cooled down, there was a single peak in the gain. In the left side of this peak the open-loop amplifier pole is in the RHP while in the right side of this peak the open-loop amplifier pole is in the LHP. This indicates that the effect of $k_1 \cdot g_{m1c}$ becomes less dominant at lower temperatures.

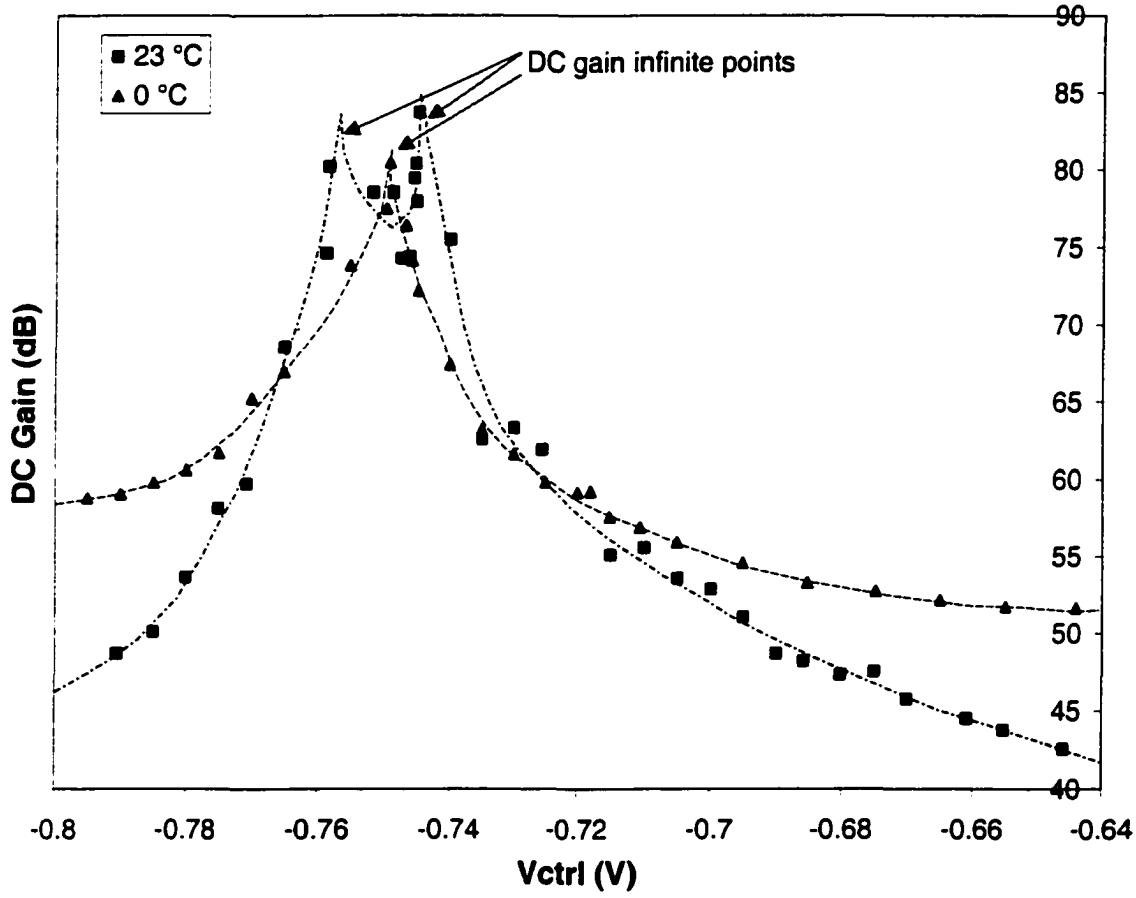


Figure 37. Measured temperature effects on the DC gain

4.3 Output Swing

The relationship between the DC gain and the differential output voltage, V_{od}, was measured by keeping the control voltage fixed. Here the DC gain is defined based on expression (94). Figure 38 shows measured output swing. The symbols are measured data. The DC gain is more than 85dB for a 100mVp-p output differential voltage. DC gain exceeds 60dB for an 876mVp-p output differential voltage.

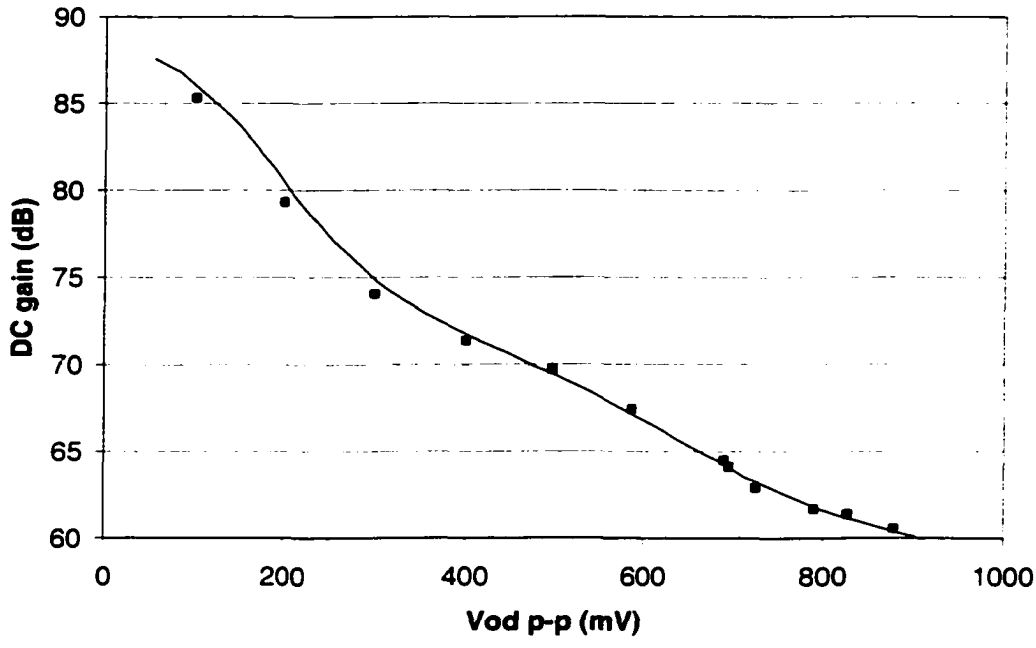


Figure 38. Measured output swing

4.4 Frequency Response

The frequency response was tested at the outputs of the feedback amplifier. The amplifier was driving one on chip output buffer, an 8pF oscilloscope probe, and the capacitance from the pads and the package at each output node. The cutoff frequency of the closed-loop amplifier was measured at 2.3MHz. Simulation results showed that a total capacitance of 80pF resulted the same closed-loop cutoff frequency.

The frequency response measurement did not provide the desired results. The frequency response of the amplifier was supposed to be measured after two on chip output buffers which are added at the outputs of the designed feedback amplifier in order to drive 10pF capacitance load. Unfortunately, the output buffer was not carefully designed. Simulation results showed that the cutoff frequency of the output buffer was less than the cut-off frequency of the feedback amplifier when the

buffer is driving the 10pF load thus masking the amplifier's actual frequency response. In addition, large parasitic capacitance (up to 5.32pF) and inductance (up to 8.18nH) introduced by the ceramic DIP40 package used to package the amplifier further reduced the cut-off frequency of the output buffer. As a result, the frequency response of amplifier could not be effectively tested as planned to obtain the frequency response of the amplifier.

4.5 Performance Summery

The power consumption for the amplifier was 31mW from a 3V supply. Most power was consumed by the second stage of the amplifier (28mW). The first stage only consumed 2.5mW. The output buffers consumed 17mW. Table 7 summarizes the measured results.

Table 7 Measured amplifier performance at the room temperature

Power supply	± 1.5 V
Technology	AMI C5N 0.5um CMOS
Area (includes buffers and feedback resistors)	0.077mm^2
DC gain	85 dB
Unity-gain frequency	2.3 MHz (see Section 4.4 for load)
Power dissipation	31 mW
Output swing	DC gain exceeds 60dB for 876mVp-p output differential voltage

CHAPTER 5. FAST SETTLING AMPLIFIER WITH FEEDFORWARD COMPENSATION TECHNIQUE

5.1 Introduction

The settling behavior of operational amplifiers plays a significant role in a wide variety of analog and mixed signal systems. These include switched-capacitor filters, sample and hold circuits, algorithmic A/D converters, pipelined A/D converters etc. The settling performance of the op amp determines the accuracy and the speed that can be reached. Many aspects of the settling behavior of operational amplifiers have been analyzed by various authors in order to improve the settling performance [48]. For example, [49] discussed the design considerations for fast-settling op amps in switched-capacitor circuits. [50] analyzed the effect of a replica-amp gain enhancement technique on the settling time of a two-stage op amp. Generally, fast-settling requires single pole settling behavior and a large gain-bandwidth product (GB) while accurate settling requires a high DC gain [31].

As discussed in Chapter 1, feedforward compensation is often used to bypass an amplifier or level translator stage that has poor high-frequency response. Also feedforward compensation techniques have been used to stabilize operational amplifiers in low voltage applications [28][29][30]. The conventional feedforward techniques use an ac bypass capacitor as the feedforward element connecting the input to the output or to intermediate output nodes. One undesirable property inherent in many feedforward compensation schemes is the existence of the slow-settling components in the step response of the amplifier. This is caused by mismatch between pole-zero pairs which results in imperfect pole-zero cancellation. Imperfect cancellation of the pole-zero pairs results in the appearance of extra decaying exponential components in the transient response. If the magnitudes of the mismatches are small, the magnitudes of the undesirable components are also small. However, if

the mismatches are large, the sizes of the undesired components are also large. Unfortunately, accurate pole-zero cancellation is not easy to ensure due to modeling errors, process variation, and environmental factors. Several feedforward techniques have been presented [26][27][28][29][30]. In these schemes, capacitors are used as feedforward elements connecting the input to the output or to intermediate output nodes. The exact pole-zero cancellation is affected by the parasitic capacitance and is not well controlled.

In fact, the feedforward path introduces zeros in the open-loop transfer function that can be used to shape the overall frequency response typically by using the zeros for pole-zero cancellation. If the LHP zeros introduced by the feedforward path are designed to cancel the low frequency poles of amplifiers, the bandwidth of the amplifier can be greatly extended.

In this work, a new feedforward compensation amplifier architecture that provides very fast settling performance is introduced. A feedforward path that has a bandpass characteristic is added to a conventional amplifier. The LHP zeros are designed to exactly cancel with the lowest-frequency pole. As a result, the unity-gain frequency of the amplifier is greatly extended and an effective single pole response is achieved. Design formulas are derived for exact pole-zero cancellation. Simulation results show that the proposed amplifier structure has the potential to achieve a large unity-gain bandwidth and fast settling performance.

5.2 Proposed Fast Settling Amplifier Architecture

Figure 39 shows the block diagram of the proposed fast-settling amplifier structure. The baseband path is denoted by a high gain amplifier with gain A(s) and the feedforward path is denoted by a bandpass filter with gain H(s). The compensated amplifier gain is given by

$$Ac(s) = A(s) + H(s) \tag{95}$$

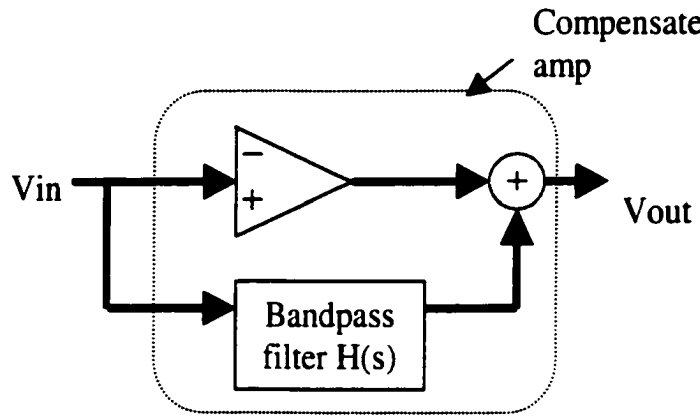


Figure 39. Block diagram of the proposed amplifier

Assume the basic amplifier A(s) is a single-pole amplifier that can be modeled by the transfer function

$$A(s) = \frac{A_0}{(1 + \frac{s}{\omega_{p1}})} \tag{96}$$

where A_0 is the DC gain and ω_{p1} is the bandwidth of the basic amplifier. Assume the bandpass filter is second-order modeled by the transfer function

$$H(s) = \frac{H_0 \frac{\omega_0}{Q} s}{(s^2 + \frac{\omega_0}{Q} s + {\omega_0}^2)} \tag{97}$$

where H_0 is the peak gain, ω_0 is the center frequency, and Q is the Q-factor of the bandpass filter.

From (95), the transfer function of the compensation amplifier is given by

$$A_c(s) = A(s) + H(s) = \frac{A_0}{(1 + \frac{s}{\omega_{p1}})} + \frac{H_0 \frac{\omega_0}{Q} s}{(s^2 + \frac{\omega_0}{Q} s + {\omega_0}^2)} \tag{98}$$

The DC gain of the compensated amplifier remains the same as that of the basic amplifier. However, pole locations are changed and zeros are introduced by the feedforward path.

$$P1 = -\omega_{p1} \tag{99}$$

$$P2 = \frac{\omega_0}{2Q}(-1+\sqrt{1-4Q^2}) \tag{100}$$

$$P3 = \frac{\omega_0}{2Q}(-1-\sqrt{1-4Q^2}) \tag{101}$$

The two zeros of the compensated amplifier are given by

$$z_{1,2} = \frac{\omega_0}{2(A_0\omega_{p1}Q + H_0\omega_0)}(-A_0\omega_{p1} - H_0\omega_{p1} \pm \sqrt{A_0^2\omega_{p1}^2 + 2A_0\omega_{p1}^2 H_0 + H_0^2\omega_{p1}^2 - 4A_0^2\omega_{p1}^2Q^2 - 4A_0\omega_{p1}QH_0\omega_0}) \tag{102}$$

The position of the first pole is determined by the bandwidth of the basic amplifier while poles P2 and P3 are totally depended on the design parameters of the bandpass filter.

Assume ω_{p1} is the lowest-frequency pole so that the basic amplifier does not require a wide-bandwidth. $z_{1,2}$ can be designed so that z1 cancels with ω_{p1}. Different relationships can be used to achieve this pole-zero cancellation. One convenient way is to make the two zeros coincident and equal to P1. Equation (103) and (104) express the parameter relationships needed for this type of pole-zero cancellation.

$$\omega_{p1} = \frac{\omega_0\omega_{p1}}{2(A_0\omega_{p1}Q + H_0\omega_0)}(A_0 + H_0) \tag{103}$$

$$\sqrt{A_0^2\omega_{p1}^2 + 2A_0\omega_{p1}^2 H_0 + H_0^2\omega_{p1}^2 - 4A_0^2\omega_{p1}^2Q^2 - 4A_0\omega_{p1}QH_0\omega_0} = 0 \tag{104}$$

A manipulation of the above equations gives the following simpler but equivalent relationships

$$Q \le 0.5 \tag{105}$$

$$H_0 = A_0\sqrt{1-4Q^2} \tag{106}$$

$$\omega_0 = \frac{2Q\omega_{p1}}{1-\sqrt{1-4Q^2}} \tag{107}$$

If the above conditions are met, actually the two coincident LHP zeros will exactly cancel P1 and P2. This reduces the amplifier to a single pole amplifier with pole P3. It is observed that the bandwidth of the compensation amplifier will be

$$BW = -P3 = \frac{1+\sqrt{1-4Q^2}}{1-\sqrt{1-4Q^2}}\omega_{p1} \tag{108}$$

For Q<0.5, the bandwidth of the compensated amplifier will be larger than that of the basic amplifier. According to the derivation in [31], the compensated amplifier will have faster settling behavior than the basic amplifier.

The goal is to increase the compensated amplifier's bandwidth as large as possible. Based on equation (108), this means a small Q should be picked. Although a small Q will result in a larger compensated amplifier bandwidth, this will require a high gain and high resonant frequency for the bandpass filter in the feedforward path. Figure 40 shows the bandwidth enhancement ratio ω_{com}/ω_{p1}

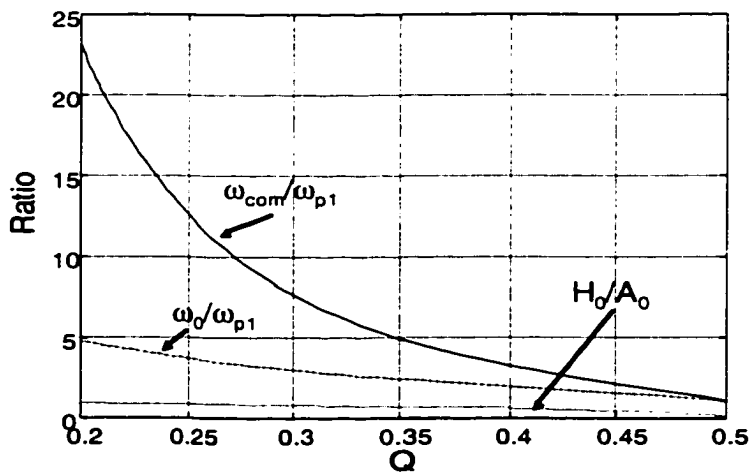


Figure 40. Bandwidth and gain relationship with Q

and the gain and ω_0 requirements for the bandpass network when Q changes. This plot shows the trade-off that must be considered when choosing Q of the bandpass network.

5.3 Simulation Results

In order to verify the settling performance of the proposed feedforward amplifier architecture, preliminary simulation results for a unity gain feedback amplifier using a conventional single-pole amplifier are compared with the same amplifier that has bandpass gain enhancement. Simulations were performed on a "10-bit" amplifier using Matlab. The basic amplifier should provide sufficient DC gain to ensure the required settling accuracy. For a "10-bit" performance, a minimum DC gain of 1000 will achieve 0.1% settling accuracy for a unity-gain feedback configuration. As a design example, the DC gain of the basic amplifier was chosen to be 2,000. The bandwidth of the basic amplifier was chosen to be 3.5KHz. A pole Q of 0.2 which satisfies (105) was selected. H_0 and ω_0 were determined to be 1833 and 16.776kHz respectively based on equations (106) and (107).

The open-loop frequency response and the unity gain close-loop frequency response of the basic amplifier and the compensated amplifier are shown in Figure 41 and Figure 42. The

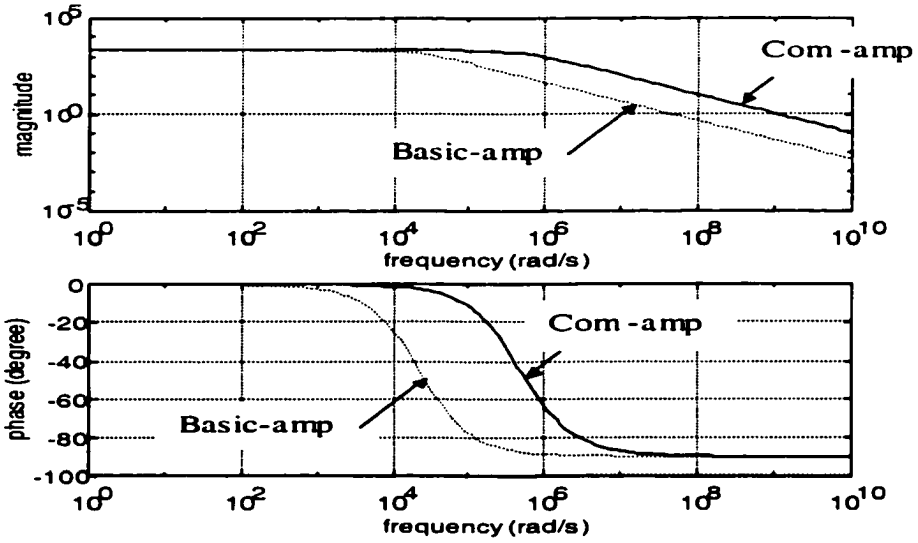


Figure 41. Open-loop frequency response

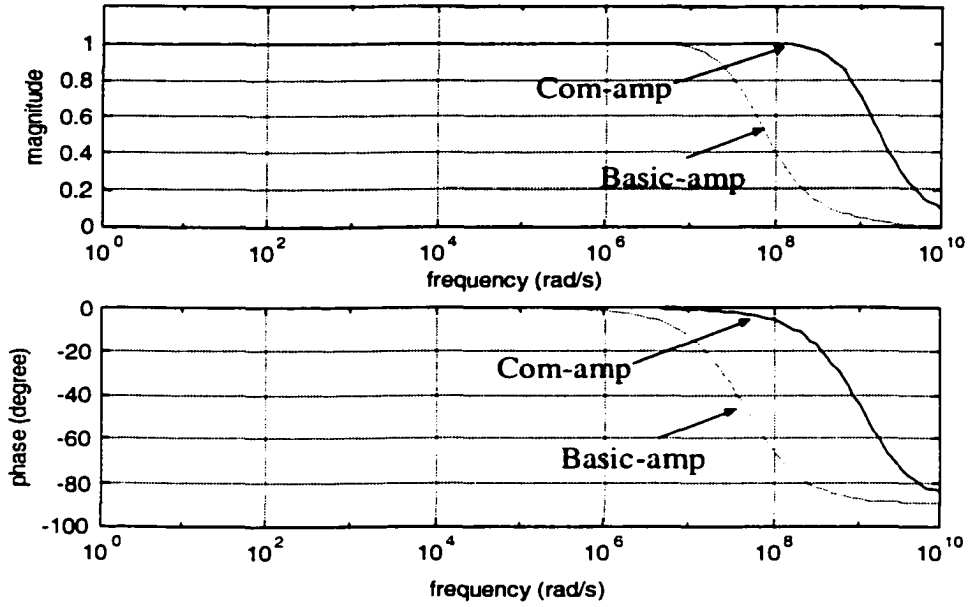


Figure 42. Unity-gain close-loop frequency response

compensated amplifier has a single-pole response and its unity-gain bandwidth is much larger than that of the basic amplifier.

Table 8 shows the unity-gain frequency, ω_t, of the basic amplifier and the compensated amplifier for ω_0= 16.776kHz, H_0=1833 and Q=0.2. The Unity-Gain frequency of the compensated amplifier is increased by 23 times.

Table 8 Bandwidth comparison of compensated and uncompensated amplifier.

	Basic amplifier	Compensated amplifier
DC gain	2000	2000
Unity-gain frequency	7MHz	161MHz
Phase margin	90 degree	90 degree

Figure 43 shows the unity-gain step responses of the basic amplifier and the compensated amplifier to a 1-V input step. Figure 44 shows details of settling behavior at the 0.1% accuracy level. Table 9 summarizes the unity-gain step responses to a 1-V input step. Compared to the basic amplifier, it is clearly shown that the compensated amplifier has much faster settling performance.

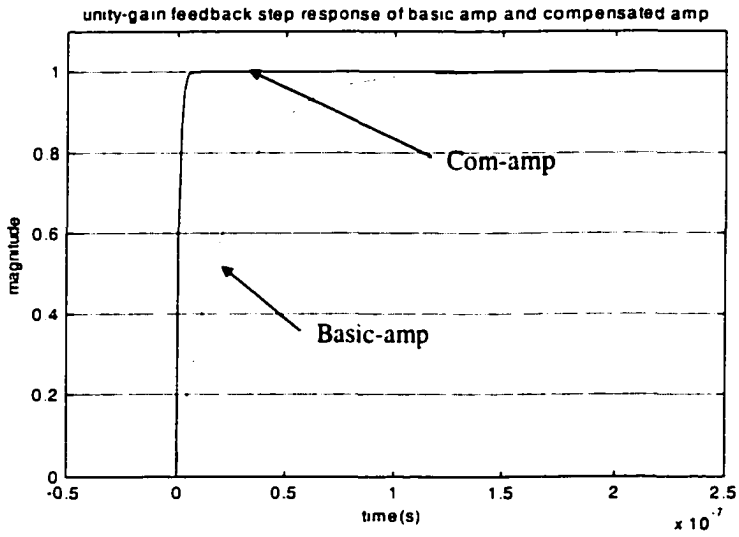


Figure 43. Step response

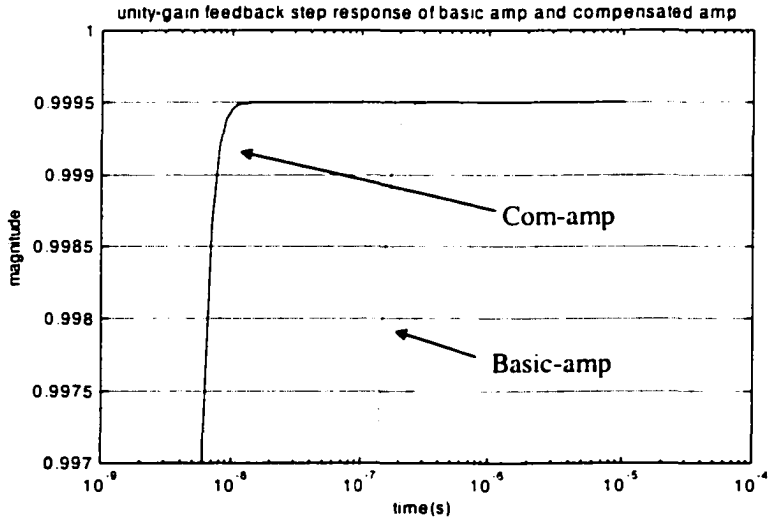


Figure 44. Step response with expanded voltage scale

Table 9 Transient response summery

Time (ns)	Basic amplifier	Compensated amplifier	Improvement ratio
Rise time (10% - 90%)	50.1	2.1	23.86
2% settling time	89.4	3.8	23.53
1% settling time	105.7	4.6	22.98
0.2% settling time	147.6	6.4	23.06
0.1% settling time	172.6	7.5	23.01

Pole-zero mismatch plays an important role in high accuracy settling performance. Imperfect pole-zero cancellation always introduces an additional settling term [4]. Since the proposed compensation technique cancels a low frequency pole, the imperfect pole-zero cancellation will introduce a long time constant which is generally referred to as a slow settling time constant. The slow settling time constant by itself, however, is not of concern. What is of concern is the magnitude of the resulting slow settling component in the output. If the magnitude of this slow settling component is sufficient small, the settling time of the compensated amplifier will be very fast. The robustness of the compensation technique must be considered to determine whether the improvements predicted in the simulations can be realistically achieved.

In order to test the robustness of the proposed amplifier structure, the design parameters H_0, ω_0 and Q of the bandpass filter were all varied by ±10% from their ideal design values and the compensated amplifier's settling behavior was observed. These variations are defined as:

Case 1: the basic amplifier,

Case 2: nominal H_0, Q, ω_0

Case 3: H_0 increased by 10%

Case 4: H_0 deceased by 10%

Case 5: ω_0 increased by 10%

Case 6: ω_0 decreased by 10%

Case 7: Q increased by 10%

Case 8: Q decreased by 10%

Case 9: H_0 decreased by 10%, Q increased by 10%, and ω_0 decreased by 10%.

Figure 45 shows the comparison of the settling time performance of the basic amplifier and the

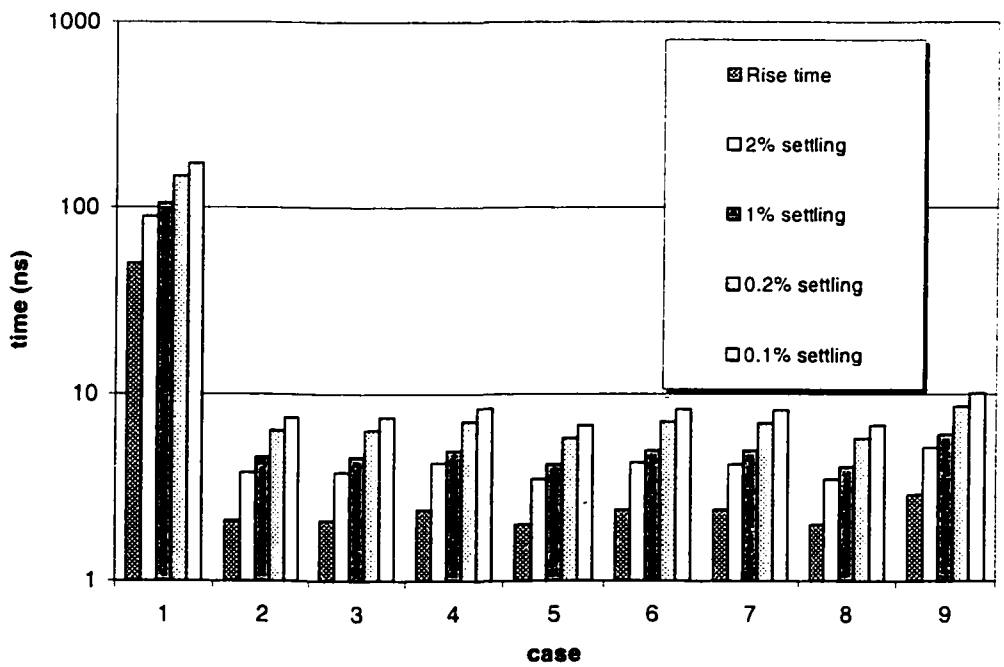


Figure 45. Comparison of the settling performance

compensated amplifier when the design parameters of the bandpass are changed. This figure shows the rise time, and the time required for 2%, 1%, 0.2%, and 0.1% settling for various cases.

Figure 45 indicates the design robustness of the compensated amplifier. Significant improvement in rise time and settling behavior is achievable even though the design parameters of the bandpass filter have a large variation.

5.4 Conclusion

A new amplifier architecture that uses bandpass feedforward compensation is presented. It is shown that a feedforward path that has a bandpass characteristic can be used to significantly extend the unity-gain-frequency of the overall amplifier. By choosing the proper gain, resonant frequency, and Q factor for the bandpass filter, the zeros can be placed on the top of the poles eliminating the slow-settling component. Simulation results predicted significant improvements in rise time and settling performance and demonstrated that the bandpass compensation scheme is reasonable robust.

CHAPTER 6. AN ASYNCHRONOUS DATA RECOVERY/RETRANSMISSION TECHNIQUE WITH DELAY-LOCKED LOOP

6.1 Introduction

In serial communication systems, the clock information is embedded into the data stream and is not transmitted separately. The recovery of serial data is a non-trivial problem since it is transmitted asynchronously and is corrupted with timing jitter and noise. Synchronization has to be achieved at the receiver end. Further, due to finite clock tolerances, there might be frequency differences in the clocks at two different transceivers, which would generate underflow or overflow if the data has to be retransmitted at different points of the network using local clocks. Therefore, data recovery and retransmission plays a crucial part in communication at the physical layer. Data recovery perform the following functions:

- Extract timing information from the incoming data
- Accurately read data with reduced jitter
- Retransmit data with reduced jitter

The demand for high speed serial-data communication networks motivates research on low-cost low power data recovery circuits. Most existing commercial high speed serial data recovery techniques are based on using a local voltage controlled oscillator (VCO) and a phase-locked loop (PLL) to generate a recovered clock which is used to sample the incoming data [36][37][38][39] [54][55]. Two fundamental limitations of such PLL-based data recovery systems are the long acquisition time required for locking onto the incoming data and susceptibility to jitter on the incoming data. Data recovery systems generally have to contend with the conflicting requirements of

fast acquisition time and immunity to internal noise. Especially, in the case of PLL based recovery systems, the loop filter bandwidth has to be selected as a compromise between the two requirements.

The history of the DLLs is relatively young compared with that of the PLL. Since it is similar to the phase locked loop in many ways and it is simpler, there is not much literature on the system level analysis of such system. However, this does not prevent its wide application in modern monolithic systems. A rather specific introduction to DLL can be found in [56]. The block diagram of a Delay-Locked Loop is shown in Figure 46. The main deference between a PLL and a DLL is the presence of a Voltage Controlled Delay Line (VCDL) in a DLL, as opposed to a Voltage Controlled Oscillator (VCO) in a PLL.

The VCDL produces a phase-shifted version of the input, the phase shift or delay being dependent on the control voltage applied to it. The reference input V_{in} is not only fed into the phase detector, but is also fed into the delay line. The output from the delay line is aligned to the input by the feedback loop. The basic ideal is that if the input is periodic and the delay through the VCDL is a multiple of the input time period T, the phase shift through the VCDL can be considered zero. When the DLL is in lock, the total delay between the output and the input is exactly nT, no skew exists.

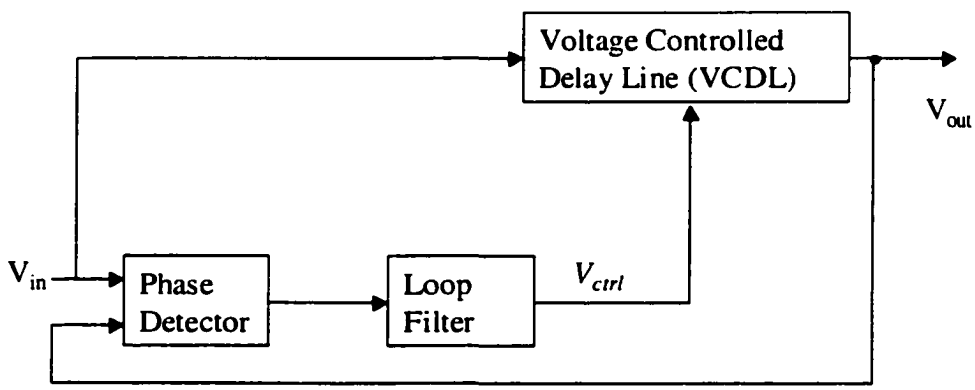


Figure 46. Block diagram of a DLL

Thus, a constant phase difference is maintained between the input and the output of the VCDL through a constant control voltage. The DLL does not create a new signal but only delays the input reference signal. This feature of the DLL gives it some unique attributes.

The linearized s-domain model for analyzing DLLs is shown in Figure 47. There is no integration in the DLL but just a constant gain K_{VCDL}. There is no stability problem in DLL either. A simple capacitor C is enough to serve as the loop filter. The phase transfer function is:

$$H(s) = \frac{\phi_o(s)}{\phi_i(s)} = \frac{K_{PD}K_{VCDL}F(s)}{1 + K_{PD}K_{VCDL}F(s)} = \frac{\frac{K_{PD}K_{VCDL}}{C}}{s + \frac{K_{PD}K_{VCDL}}{C}} \tag{109}$$

Three observations can be drawn from equation 109: (1) DLL is a phase low pass filter. It can suppress the jitter in the input. (2) The order of the transfer function of the DLL is that of the loop filter. If a simple capacitor C is used as the loop filter, DLL is a first order system. This gives a more relaxed trade-off between gain, bandwidth, and stability. (3) Since noise injected into a VCDL is flushed out at the end of it whereas it is recirculated in a VCO, the jitter contribution by a DLL is much lower that that by a PLL.

Since a delay line does not generate a signal, DLL is mainly applied as clock and timing generator where frequency synthesis is not needed. The applications of DLL include generating

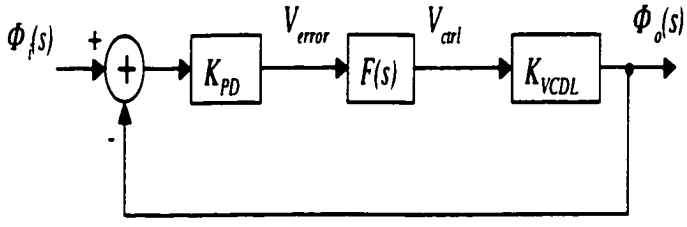


Figure 47. Linearized s-domain model of DLL

clocks of different phases clock generator for microprocessor and DRAM [57], and precise delay generation for oversampling [58][59], etc..

In data recovery circuits, some architectures have been proposed using DLL's. These structures either use a DLL to recover clock information that has been transmitted along with the data, or align a local clock with the incoming data [60][61].

In our work, a new data recovery/retransmission technique for use on the 1.0625 Gbaud fibre channel is proposed [62][63]. This technique is asynchronous in nature, is highly insensitive to incoming jitter and requires zero acquisition time.

This chapter will introduce the proposed data recovery/retransmission technique. The research work focuses on investigation of one of the key requirements of the asynchronous data recovery technique; here is a delay cell with accurate delay control and no data dependency.

6.2 An Asynchronous Data Recovery/Retransmission Technique

The data recovery technique that is used and the design considerations depend on the characteristics of the data being transmitted. Binary data is most commonly transmitted in the Non-Return to Zero (NRZ) format. Here, a binary '1' is transmitted at one amplitude and a '0' at another. The amplitudes are chosen based on Signal-to-Noise Ratio (SNR) requirements and the properties of the channel. The maximum frequency of the transmitting data stream is 1/Td, where Td is the bit period. This is one-half the transmitting clock frequency and therefore the channel bandwidth requirements are eased. NRZ coding systems are set up to guarantee a certain number of transitions in a particular time interval for clock synchronization. In addition, transitions help maintain a constant DC level ad prevent charge build-up in the system. An example of a coding system that has found widespread popularity is the 8B/10B encoding scheme. This scheme is used on the Gigabit Ethernet

and Fibre channel. DC balance is maintained by ensuring that the number of 0's and 1's in every consecutive two symbols is equal. This results in a maximum of 5 consecutive 0's or 1's in the data stream. This property is exploited in proposed asynchronous data recovery technique.

Consider incoming data with a nominal bit period T_d passing through a delay line as illustrated in Figure 48. If delay stages having an accurate delay of $T=T_d$ are available, and the cumulative effects of input jitter at the output of the delay line is small compared to T, the data in the delay line will be read accurately when it is sampled T/2 second after an input transition.

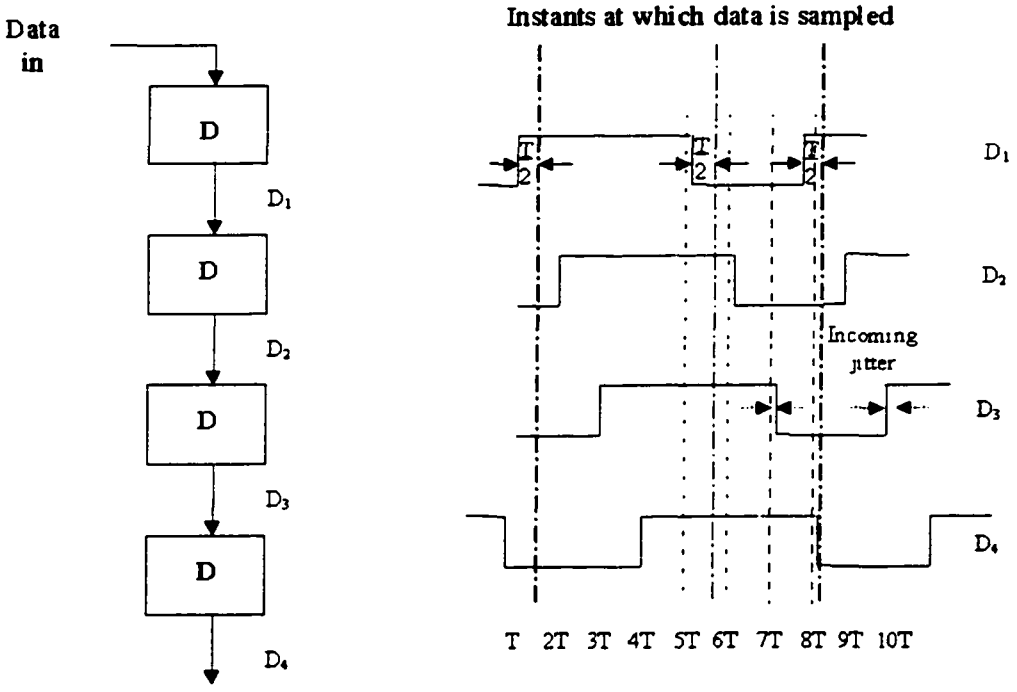


Figure 48. Reading data using data transition

A new technique for asynchronous data recovery based upon using a delay line in the incoming data path is proposed [62]. This technique recovers the incoming data without recovering a clock signal. The system level diagram of an asynchronous data recovery/retransmission circuit is shown in Figure 49. A background DLL is locked onto the local clock frequency 1/Tc and generates precise delays in the VCDL. The incoming data with a nominal bit period Td is rippled through the VCDL. The number of delay cells in VCDL is greater than or equal to the maximum number of consecutive zeros and ones in the incoming data stream. If the incoming data is read into the data buffer Td/2 after every data transition, then all incoming data can be recovered from the samples of the outputs of the delay line. When incoming data transition are closer together than the total length of the VCDL, some data points may be sampled more than once on successive data transitions. Simple logic circuitry purges any redundant samples and sequentially places the recovered data into memory [63]. Since recovery of the data is done asynchronously, retransmission is not instantaneous.

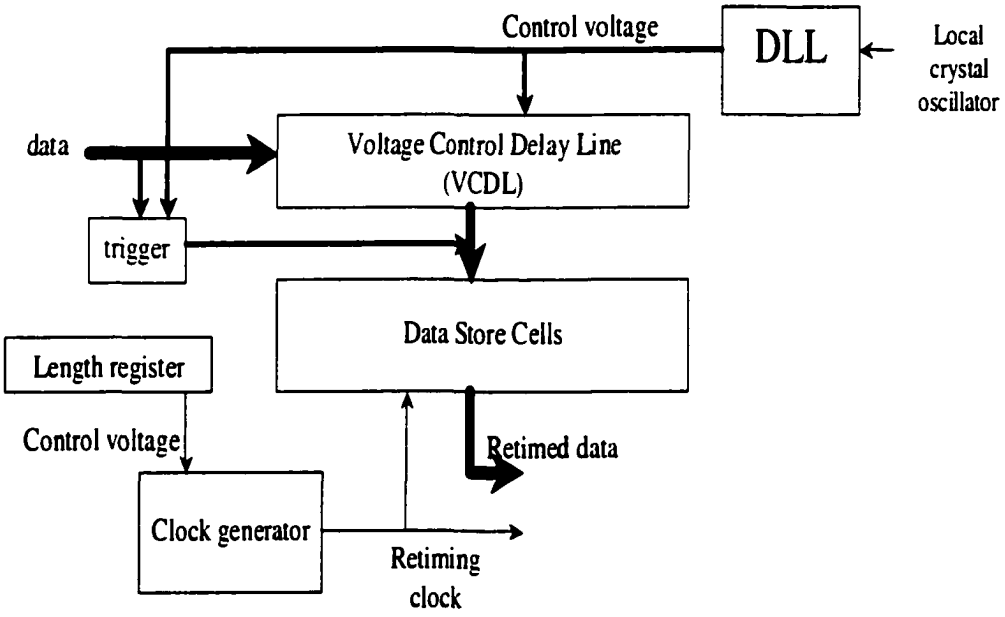


Figure 49. System level diagram of asynchronous data recovery technique

If data retransmission is required, a retiming clock, initially referenced from the local clock, is used. Due to the latency of the system, phase alignment is not needed. However, tolerances between the transmitting and receiving clock can lead to memory underflow or overflow. Thus, the frequency of the retiming clock needs to be adjusted based on the depth of the data buffer.

This system offers distinct advantage over PLL-based data recovery systems. First, the acquisition time on this system is zero, which means that all transmitted data can be recovered. This happens because the background DLL is already locked onto the system clock and no further information is required from the incoming clock for synchronization. Further, since the incoming data initiates the sampling function, the receiver is insensitive to accumulated jitter on the incoming data. Finally, since the retiming clock is isolated from the incoming data, the jitter on the retimed data is very low and independent of incoming jitter.

Two key performance characteristics must be satisfied for successful operation of this system. First, the delay T of the delay line must be very close to T_d. Secondly, the delays in each stage must be equal and independent of the input data sequence.

The first characteristic is readily achievable in tight tolerance channels. Specifically, a DLL can be used to lock the delay of a programmable delay cell to a crystal reference signal that is generally available in tight tolerance channels. If matching of the delay cells in the DLL to those in the signal path delay stage is achieved, the delay in the signal path delay stages will also be locked to the crystal reference. In a tight tolerance channel, this delay can be maintained to be very close to the bit period of the incoming data T_d, with only a small accumulated time error due to propagation through the signal delay line, provided the number of delay stages is not too large. The referenced DLL in the control loop inherently has small jitter and since it is not in the signal path, it can be put in

a sleep mode once the correct delay has been established. It need only be reactivated at power up or when temperature changes become sufficiently large so as to cause a problematic change in delay.

The second concern is that of data dependency which could lead to increased jitter in the delayed stream resulting in increased bit error rates, or even loss of data bits. Delay cells with minimal data dependency can be designed to address the second concern. Next we will address implement of delay cells that satisfies these requirements.

6.3 Data Independent Delay Cells

One of the key requirements of the asynchronous data recovery technique proposed here is a delay cell with no data dependency. Most of the standard delay cells in use have loads that go deeply into saturation on the application of a string of continuous 0's or 1's. This is not a problem in PLL's since they deal with clock pulses having a duty cycle of 50 %; but for this technique, which requires delays up to 5 T, a delay cell with no data dependent degeneration is essential.

A fully differential delay cell is shown in Figure 50. The circuit sinks and sources the same amount of the current into load capacitance (the input capacitance of the next stage) resulting in equal

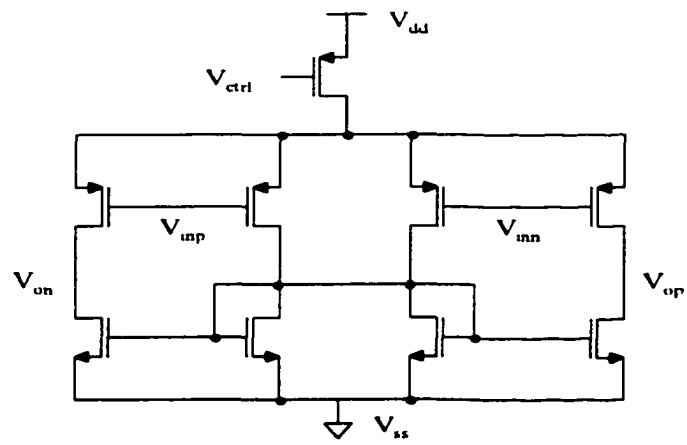


Figure 50. Differential delay cell

rise and fall time through the delay line. The control voltage V_{ctrl} controls the current available to charge or discharge load capacitance. Large values of V_{ctrl} allow a small current to flow, producing a large resistance and a large delay. The circuit has a better power supply noise rejection because of the symmetry.

The circuit is simulated with TSMC 0.35um process using the simulator HSPICE for use on the 1.0625 Gbaud fibre channel. To check that pulses are not lost by propagation through a delay line, 28 delay cells were connected, and the signals at their outputs were observed. The results are shown in Figure 51. V_{out4}, V_{out8}, and V_{out16} are the outputs at the 4^{th}, 8^{th}, and 16^{th} delay stages respectively. As

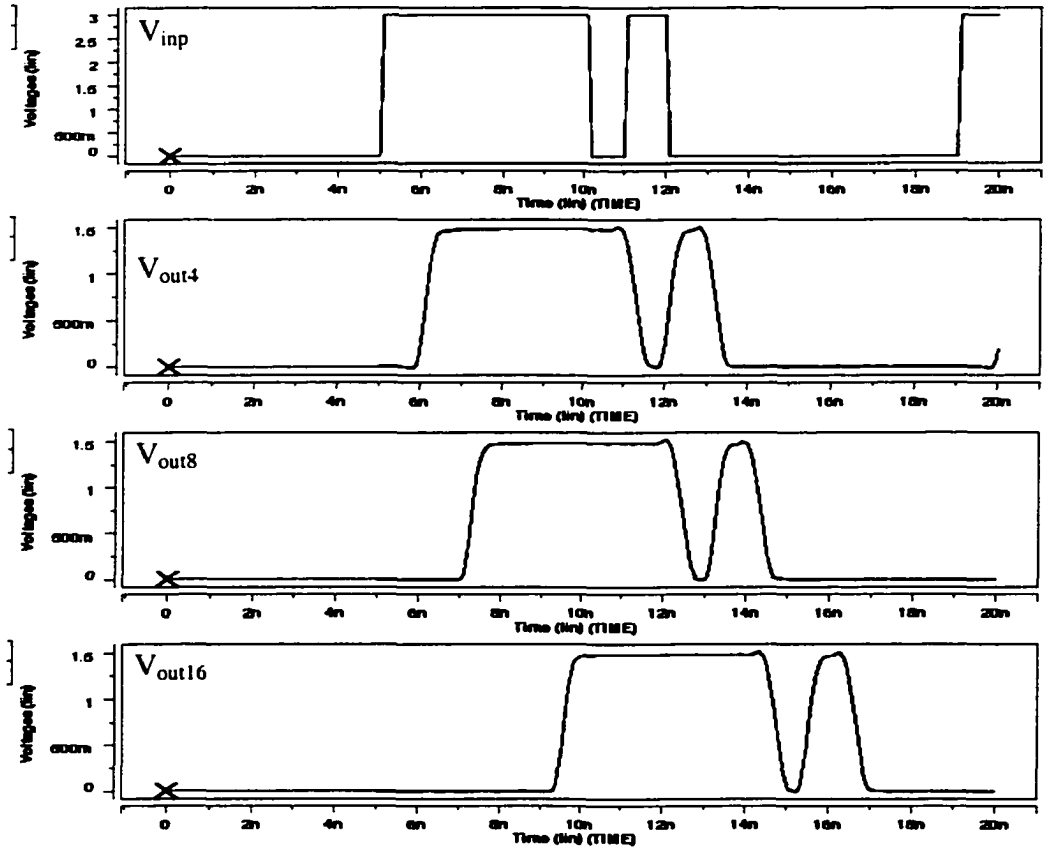


Figure 51. Simulation results for the delay cell

can be observed, the pulse widths of the 1 and 0 pulses do not appear to have deviated from each other. By varying V_{ctrl}, the variation in delay due to the variation in V_{ctrl} can be determined. Figure 52 gives a graphic result shown the relationship between the control voltage and average delay per stage. The results indicate that the delay cell has a high sensitivity and operation range, and is suitable for use in the Voltage Delay Controlled Line.

In order to evaluate power supply noise rejection behavior of the delay cell, a 100mV pulse signal is in series with a 3 Volts DC voltage as the power supply. The delays per stage versus the control voltage V_{ctrl} for power supply with and without noise are plotted in Figure 53. Curve 1 is the delay per stage for a 3 Volts DC supply. Curve 2 is the delay for a 3 Volts DC plus a 100mV pulse supply. In addition, the relative delay error due to the supply noise is shown in Figure 54. Figure 54 indicates the delay cell has good power supply noise rejection and the delay error is less than 2.6%.

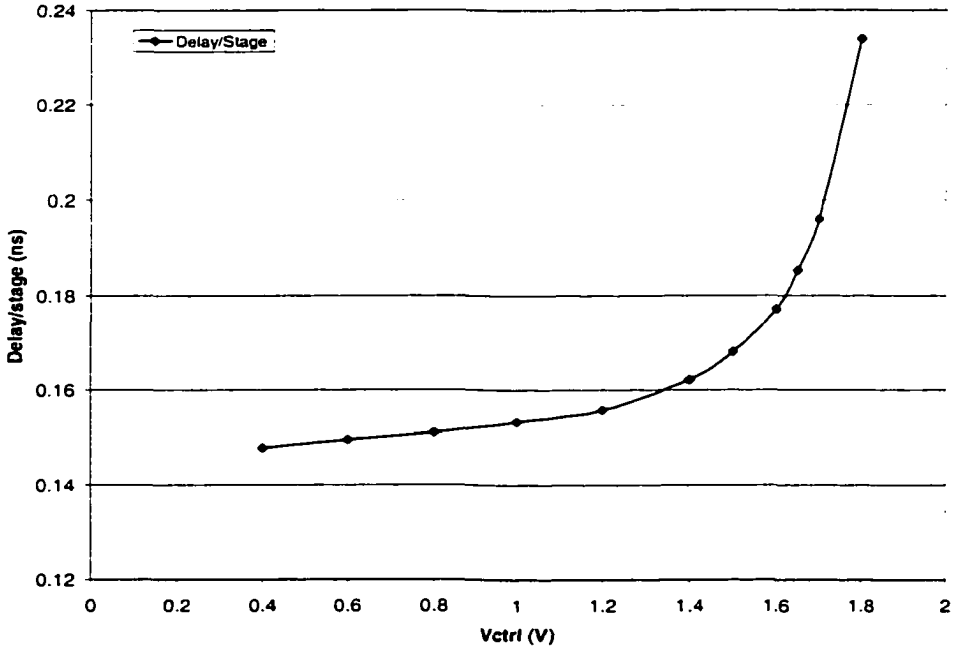


Figure 52. Delay cell performance for 3 V DC supply

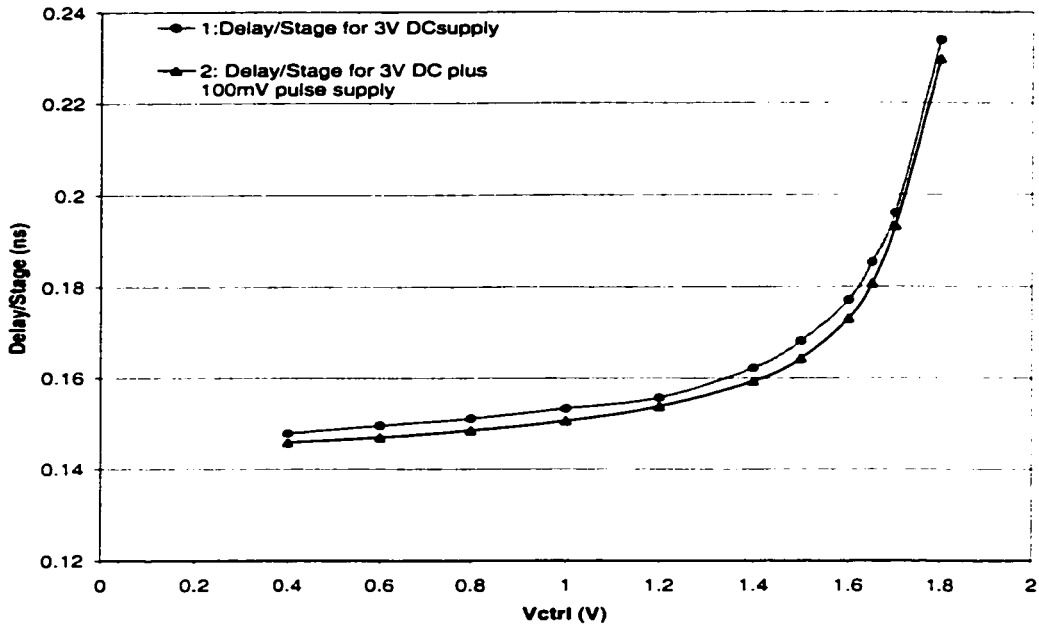


Figure 53. Delay cell performance for 3 V DC plus 100mV pulse supply

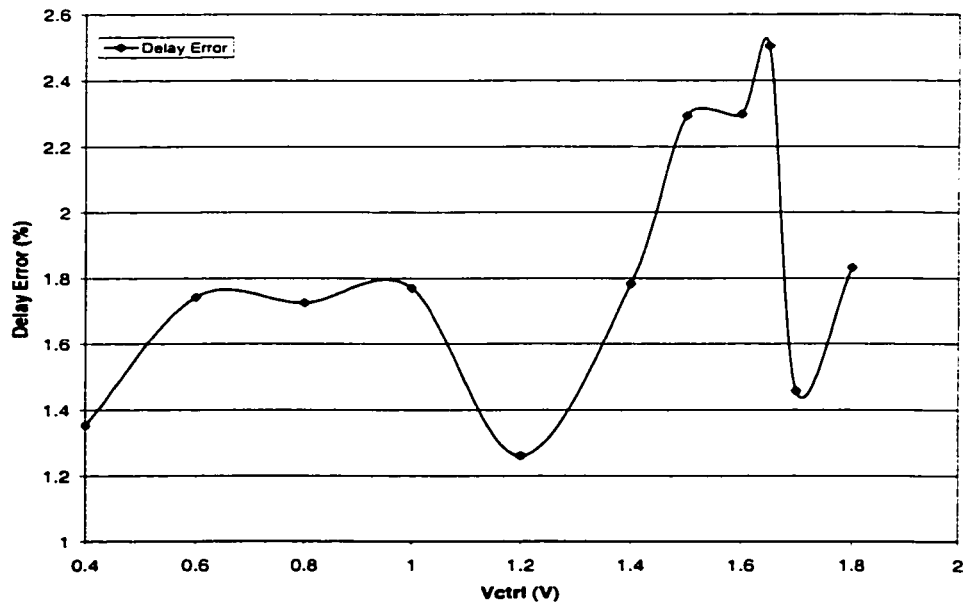


Figure 54. Delay error

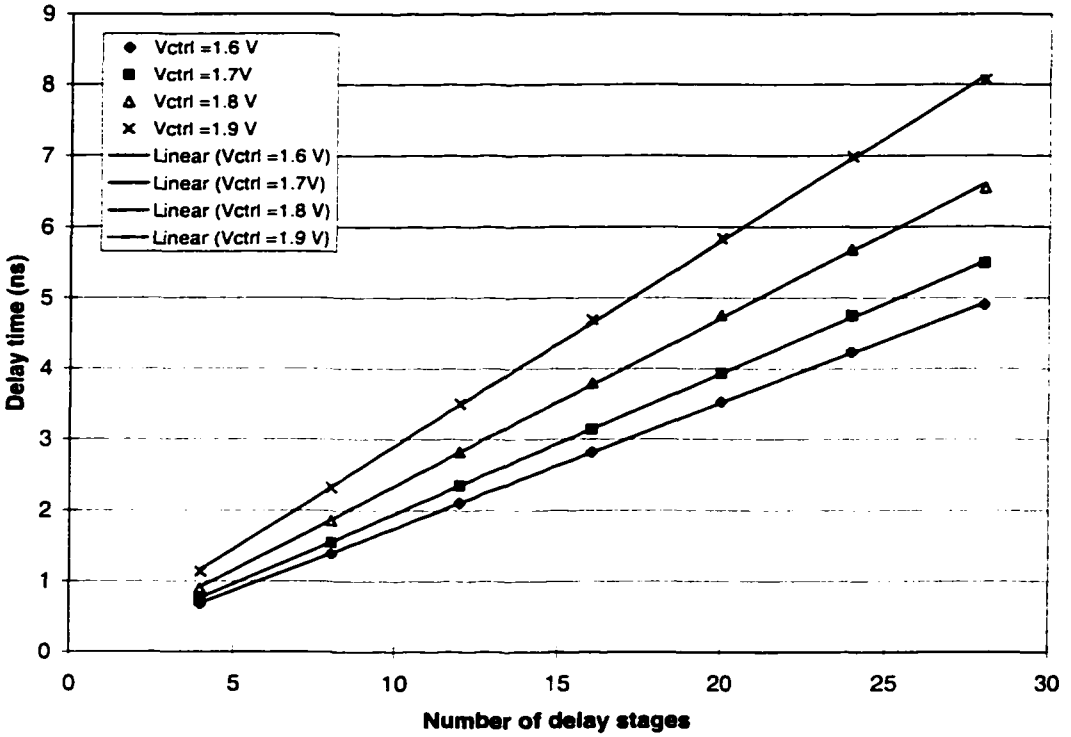


Figure 55. Delay cell performance

For a fixed control voltage V_{ctrl}, the delay after the 4^{th}, 8^{th}, 12^{th}, 16^{th}, 20^{th}, 24^{th}, 28^{th} stages are measured and plotted in Figure 55. The delay cell showed very good linearity.

In order to evaluate the reliability of the delay cell, Monte carols analysis for 28-stage delay lines was performed. Table 10 summarizes the Monte Carlo simulation of the delay performance of the delay cell with a control voltage V_{ctrl} = 1.6 V. For the simulated results, Gaussian distribution in all the parameters VFBN, VFBP, K1N, K1P, Mun, and Mup of all MOS devices are used for 80 random samples. Simulation results showed that the delay variation at the outputs of the delay line is small compared to bit period Td.

Table 10 Delay cell Monte Carlo simulation results

	Delay at the 4th stage	Delay at the 8th stage	Delay at the 12th stage	Delay at the 16th stage	Delay at the 20th stage	Delay at the 24th stage	Delay at the 28th stage
Mean (ns)	0.669	1.373	2.078	2.784	3.488	4.192	4.849
Sigma (ps)	15.9	34.5	52.1	70.9	88.7	107.6	124.7
Max (ns)	0.700	1.450	2.198	2.947	3.692	4.442	5.141
Min (ns)	0.633	1.293	1.963	2.624	3.294	3.963	4.583

6.4 Conclusion

In this chapter, a new technique for asynchronous data recovery based upon using a delay line in the incoming data path is introduced. The proposed data recovery system is well suited for tight tolerance channels and coding systems supporting standards that limit the maximum number of consecutive 0's and 1's in a data stream. This system does not require clock recovery, suffers no loss of data during acquisition, has a reduced sensitivity to jitter in the incoming data and does not exhibit jitter enhancement associated with VCO tracking in a PLL. The retimed data also has a significant reduction in jitter. Design issues were discussed, and one in particular, the delay cell with minimal data dependency was exploited in details.

CHAPTER 7. CONCLUSION

7.1 Conclusions

The operational amplifier is one of the most widely used and important building blocks in analog circuit design. High gain and high speed are two important properties of op amps because they determine the settling behavior of the op amps. As supply voltages decrease when device feature sizes are reduced, the realization of high gain amplifiers with large Gain-Bandwidth-Products (GBW) has become challenging. As the operating voltages for CMOS technology will be reduced to 1.5V and below, conventional gain enhancement techniques such as cascoding will not be viable. New gain enhancement technique suitable for low voltage operation needs to be developed.

The major contribution of this dissertation is on the negative output impedance gain enhancement techniques. The negative impedacnce gain enhancement technique offers potential for achieving very high gain and energy-efficient fast-settling and is low-voltage compatible. Two important properties of amplifiers with negative impedance gain enhancement were discussed in this chapter. The first property is stability. Incorrect existing wrong perceptions regarding stability of positive feedback amplifiers were pointed out. Three open loop pole bounds were derived to ensure stability and settling performance of amplifiers with negative impedance gain enhancement. The second property discussed is the meta-stability issue. Although open loop amplifiers may have meta-stable states, practical closed loop amplifiers will not have such states indicating meta-stability is not of concern in the feedback amplifiers. A new negative conductance gain enhancement technique was proposed. The proposed circuit generates a negative conductance that is only the function of g_{ds} and is not related to g_m. Therefore, negative g_{ds} can realistically match positive g_{ds} terms and the matching requirements for achieving very high DC gain are less stringent than for the existing $-g_m$ gain

enhancement schemes. Further, the proposed circuit has potential for precise digital control of a large DC gain by exploiting the property that there is a phase reversal as the pole crosses the origin in the open-loop transfer function that can be detected. None of the existing amplifier schemes discussed and/or showed gain control ability. A prototype high gain fully differential CMOS operational amplifier was designed and fabricated based on the proposed negative conductance voltage gain enhancement technique. Experimental results which showed a DC gain of 85dB and a peak-to-peak output swing of 876mV validated the fundamental performance characteristics of this technique. In addition, the temperature and process variation effects over the DC gain were observed and discussed.

The second contribution of this dissertation is on the development of a new feedforward amplifier compensation strategy. A new amplifier architecture that uses bandpass feedforward compensation was presented. It is shown that a feedforward path that has a bandpass characteristic can be used to significantly extend the unity-gain-frequency of the overall amplifier. By choosing the proper gain, resonant frequency, and Q factor for the bandpass filter, the zeros can be placed on the top of the poles eliminating the slow-settling component. Behavioral level simulation results predict substantial improvements in rise time and settling performance and show that the bandpass compensation scheme is reasonably robust.

The third contribution of this dissertation is on a new technique for data recovery/retransmission in serial channel communication. An asynchronous data recovery based upon using a delay line in the incoming data path is introduced. The proposed data recovery system is well suited for tight tolerance channels and coding systems supporting standards that limit the maximum number of consecutive 0's and 1's in a data stream. This system does not require clock recovery, suffers no loss of data during acquisition, has a reduced sensitivity to jitter in the incoming data and does not exhibit jitter enhancement associated with VCO tracking in a PLL. The retimed data also has

a significant reduction in jitter. Design issues were discussed, and one in particular, the delay cell with minimal data dependency was exploited in details.

7.2 Recommended Future Work

With the movement to larger levels of integration in lower-voltage processes there will be even more need for high-performance op amps. The proposed negative conductance voltage gain enhancement technique can realistically achieve very high DC gain and high speed simultaneously. The prototype high gain fully differential CMOS operational amplifier validated the fundamental performance characteristics of the negative conductance gain enhancement technique. The implementation of high gain high speed amplifier with the proposed negative conductance voltage gain enhancement technique can be further improved to achieved better performance.

- The biasing scheme for negative conductance transistors can be improved to get rid off the effect of g_{mtc} and reduce the DC gain sensitivity of process and temperature variations.
- Compensation of the amplifier can follow standard lead compensation. Therefore, power consumption can be optimized.
- Low gain stage A should be implemented as a high swing amplifier so that the overall amplifier will have better output swing.
- Self-adapting of pole locations can be used to enhance the DC gain and achieve better performance.

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